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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Populate

DBG_S - Replace with board short for MP
DBG_R - Replace with lower cost component for MP
DBG_N - Install for Non-Debug Builds
DBG_D - Remove from BOM (Depopulate) for MP
DBG_T - Used for Telemetry in MP as needed
DBG_TS - Used for Telemetry in MP as needed. This part needs to be replaced with a short if telemetry is not needed.

<Variant Name>

Title:	Table of Contents	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 1 of 76	

Schematics Change History

Version	Date	Comments

CAD Note:
Default component footprint is
SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Populate

DBG_S - Replace with board short for MP
DBG_R - Replace with lower cost component for MP
DBG_N - Install for Non-Debug Builds
DBG_D - Remove from BOM (Depopulate) for MP
DBG_T - Used for Telemetry in MP as needed
DBG_TS - Used for Telemetry in MP as needed. This part
needs to be replaced with a short if telemetry is not

<Core Design>

Title:	CHANGE HISTORY-2	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
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Connector

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2 x32 @1866MHz
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2 x32 @1866MHz
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CH B

eDP

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page 37

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USB2.0(4) + USB3.0(4) page 71

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DDPC_AUXN/P

2:1 MUX

SL1_DDC_AUX_N/P

DP 3 Lane (L0, L1, L2) page 71

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Connector
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DP/ SAM
Debug UART

2:1 MUX

HPD/CONFIG1
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SAM Debug UART

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PROCHOT#

FAN Connector
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Aggregator
Microcontroller
SAM
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IR Webcam
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CSI2

Front Webcam
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CSI2

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ROHM / BU52058GWZ-E2
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Hall Effect Sensor IC Canvas
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SEN_HALL_INT_C

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Hinger Connector
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HGR2_PWR_EN/HINGER2_POS_A

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SAM reflash
image backup
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AUDIO CODEC
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Speaker Amplifier
ALC1304 page 42

Speaker
L+/-, R+/-
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DMIC1 Onboard
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Debug Conn
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18Wh
Battery
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+7.4V

Battery Charge
Controller
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128/256/512/
1024GB SSD
Full size
PCIE card

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Title:	BLOCK DIAGRAM		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: CHARIOT		Rev: 1.00
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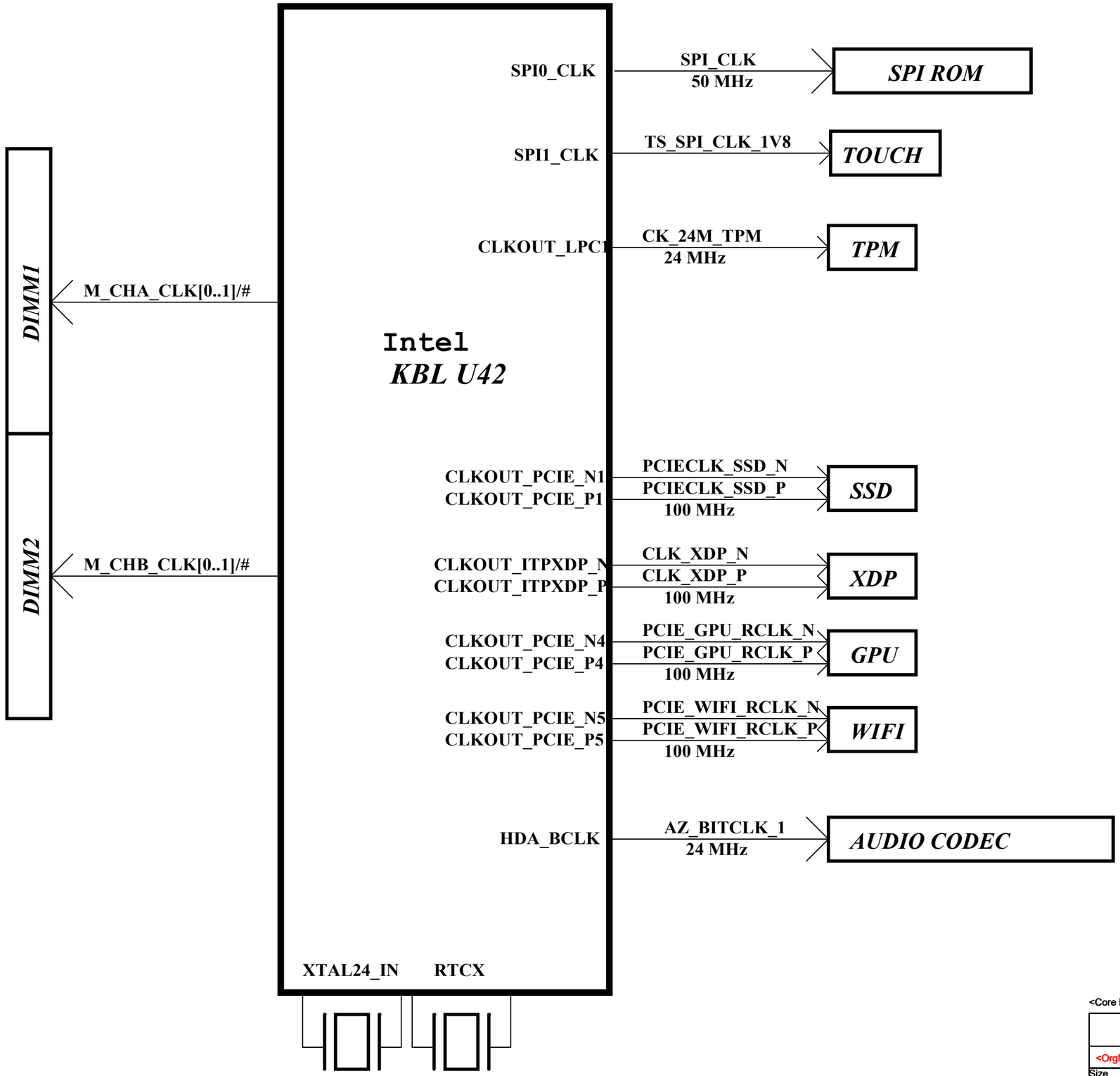
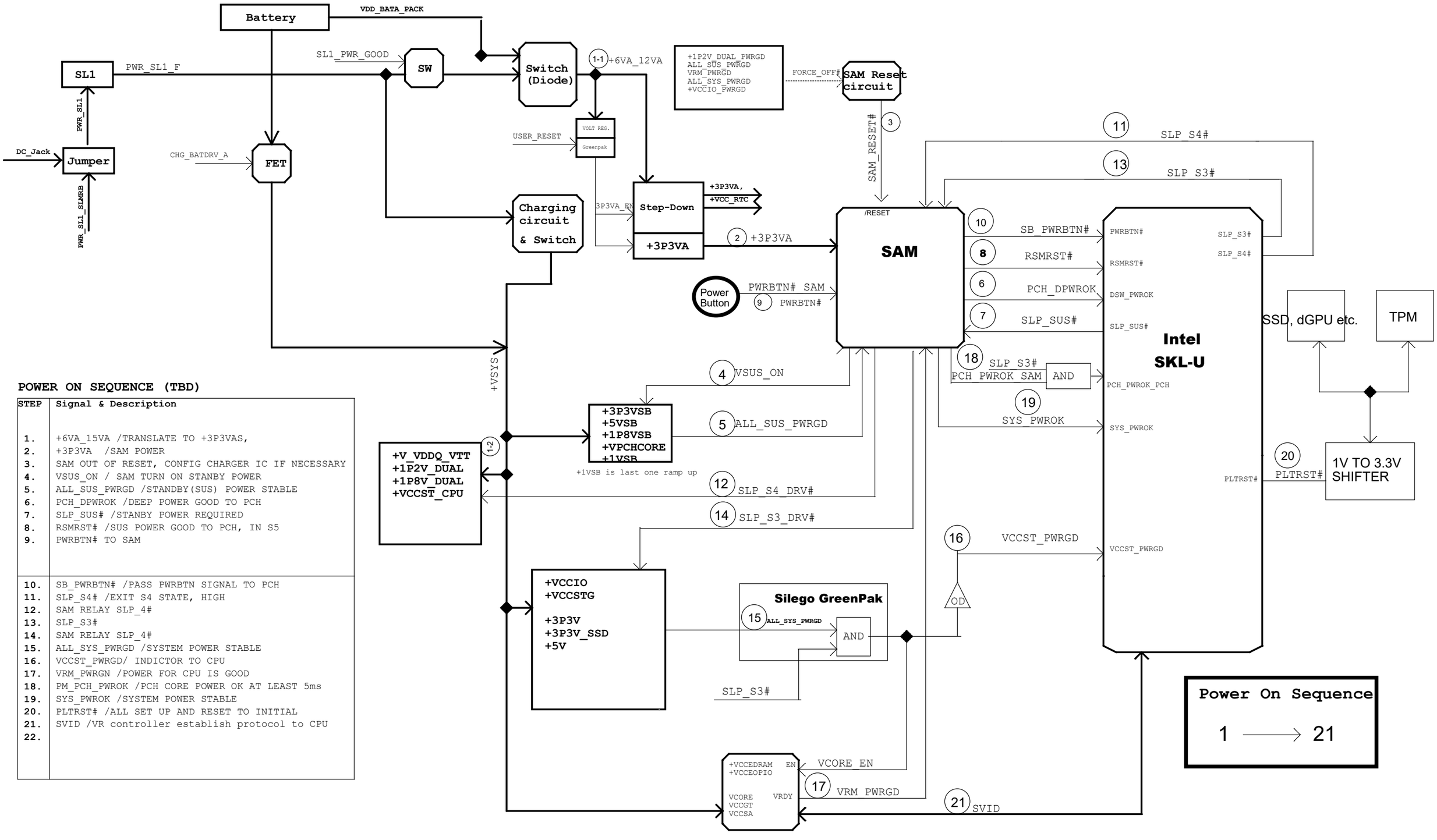


<Core Design>

Title:	CLCOK DISTRIBUTION	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 4 of 76	

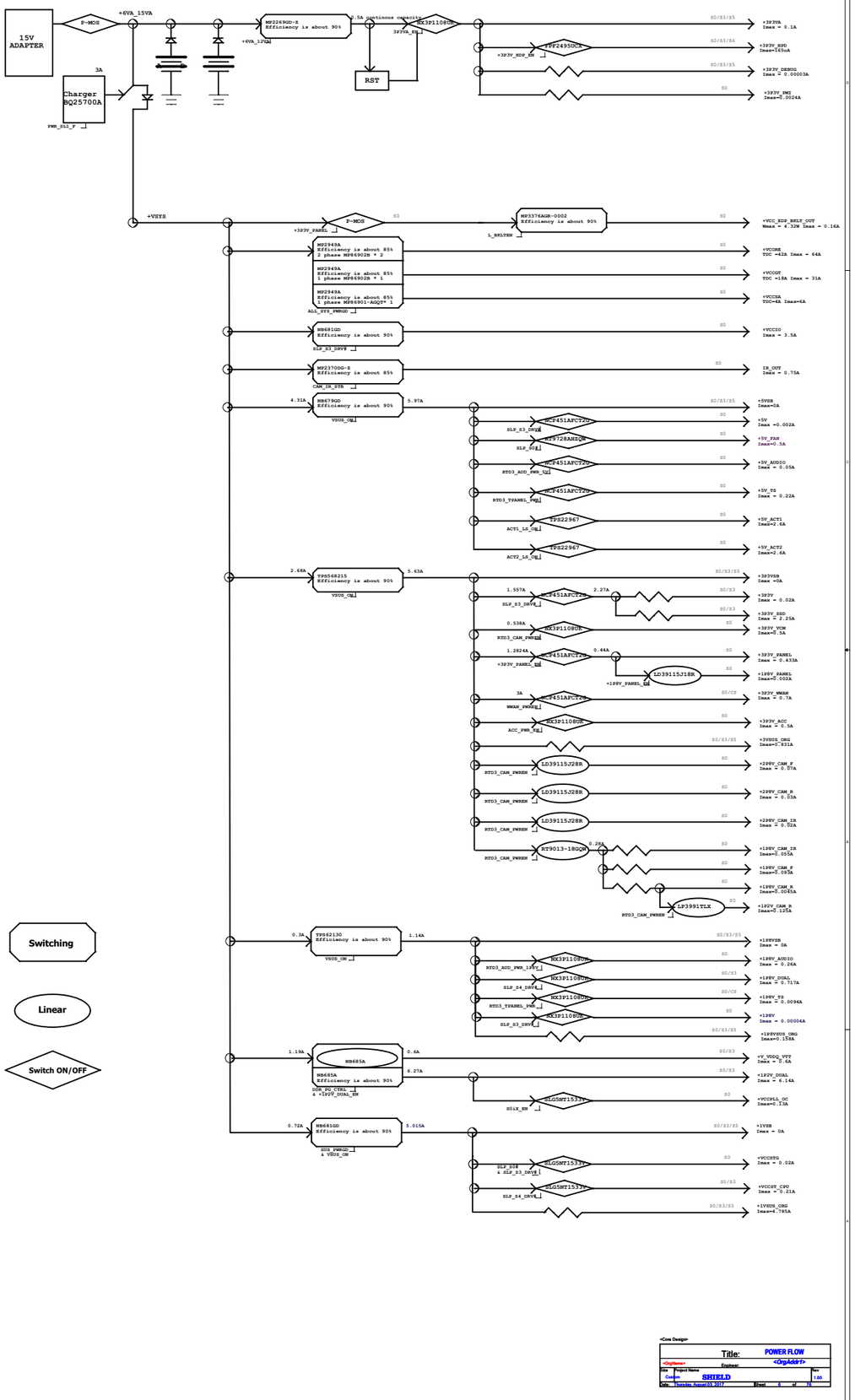


POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1.	+6VA_15VA /TRANSLATE TO +3P3VAS,
2.	+3P3VA /SAM POWER
3.	SAM OUT OF RESET, CONFIG CHARGER IC IF NECESSARY
4.	VSUS_ON / SAM TURN ON STANBY POWER
5.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	RSMRST# /SUS POWER GOOD TO PCH, IN S5
9.	PWRBTN# TO SAM
10.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
11.	SLP_S4# /EXIT S4 STATE, HIGH
12.	SAM RELAY SLP_4#
13.	SLP_S3#
14.	SAM RELAY SLP_4#
15.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
16.	VCCST_PWRGD/ INDICTOR TO CPU
17.	VRM_PWRGN /POWER FOR CPU IS GOOD
18.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
19.	SYS_PWROK /SYSTEM POWER STABLE
20.	PLTRST# /ALL SET UP AND RESET TO INITIAL
21.	SVID /VR controller establish protocol to CPU
22.	

<Core Design>

Title:	SIGNAL&RESET MAP
<OrgName>	Engineer: <OrgAddr1>
Size: A2	Project Name: SHIELD
Rev: 1.00	
Date: Thursday, August 03, 2017	Sheet 5 of 76


15V ADAPTER
P-MOS
+6VA_15VA
MP2269GD-Z
Efficiency is about 90%
+6VA_12VA
2.5A continous current
SK3P1108UC
3V3VA_EN
RST
3A
Charger BQ25700A
PWR_SRC_P
SO/S3/S5
+3P3VA
Imax = 0.1A
+3P3V_EDP_EN
SO/S3/S4
+3P3V_EDP
Imax=165uA
+3P3V_DEBUG
Imax = 0.00003A
SO
+3P3V_EMI
Imax=0.0024A
+VSYS
MP3376AGH-0002
Efficiency is about 90%
+3P3V_PANEL_EN
S_RSLTEN
+VCC_EDP_RSLT_OUT
Wmax = 4.32W Imax = 0.16A
MP2949A
Efficiency is about 85%
2 phase MP86902B * 2
+VCORE
TDC =42A Imax = 64A
1 phase MP86902B * 1
+VCCGT
TDC =18A Imax = 31A
1 phase MP86901-AGGT* 1
+VCCSA
TDC=4A Imax=6A
ALL_SYS_PWRGD
MP8681GD
Efficiency is about 90%
+VCCIO
Imax = 3.5A
SLP_S3_DRVR
MP2370DG-E
Efficiency is about 85%
+IR_OUT
Imax = 0.75A
CAM_IR_EN
4.31A
MP8679GD
Efficiency is about 90%
5.97A
VSUS_ON
+5VSB
Imax=0A
NCP451AFCT2G
+5V
Imax =0.002A
SLP_S3_DRVR
SLP_S3
+5V_FAN
Imax=0.5A
RTD3_AUD_PWR_EN
+5V_AUDIO
Imax = 0.05A
RTD3_TPANEL_PWR
+5V_TS
Imax = 0.22A
TPS22967
ACT1_LS_ON
+5V_ACT1
Imax=2.6A
ACT2_LS_ON
+5V_ACT2
Imax=2.6A
2.68A
TPS568215
Efficiency is about 90%
5.63A
VSUS_ON
+3P3VSB
Imax =0A
1.557A
2.27A
+3P3V
Imax = 0.02A
+3P3V_SSD
Imax = 2.25A
0.538A
+3P3V_VCM
Imax=0.5A
RTD3_CAM_PWREN
1.2824A
+3P3V_PANEL
Imax = 0.433A
0.44A
LD39115J18R
+1P8V_PANEL_EN
+1P8V_PANEL
Imax=0.002A
3A
WWAN_PWRGD
+3P3V_WWAN
Imax = 0.7A
ACC_PWR_EN
+3P3V_ACC
Imax = 0.5A
+3VSUS_ORG
Imax=0.831A
LD39115J28R
+2P8V_CAM_F
Imax = 0.07A
+2P8V_CAM_R
Imax = 0.03A
+2P8V_CAM_IR
Imax = 0.02A
RT9013-18GQW
0.29A
+1P8V_CAM_IR
Imax=0.055A
+1P8V_CAM_F
Imax=0.093A
+1P8V_CAM_R
Imax=0.0583A
LP3991TLX
+1P2V_CAM_R
Imax=0.125A
Switching
Linear
Switch ON/OFF
0.3A
TPS62130
Efficiency is about 90%
1.14A
VSUS_ON
+1P8VSB
Imax = 0A
RTD3_AUD_PWR_EN
+1P8V_AUDIO
Imax = 0.26A
SLP_S4_DRVR
+1P8V_DUAL
Imax = 0.717A
RTD3_TPANEL_PWR
+1P8V_TS
Imax = 0.0094A
+1P8V
Imax = 0.00004A
+1P8VSUS_ORG
Imax=0.158A
1.19A
NB685A
0.6A
+V_VDDQ_VTT
Imax = 0.6A
6.27A
+1P2V_DUAL
Imax = 6.14A
DGR_PG_CTRL
& +1V8V_DUAL_EN
SOix_EN
SLG5NT15337V
+VCCPLL_OC
Imax=0.33A
0.72A
NB681GD
Efficiency is about 90%
5.015A
SUS_PWRGD
& VSUS_ON
+1VSB
Imax = 0A
SLP_S5#
& SLP_S3_DRVR
+VCCSTG
Imax = 0.02A
+VCCST_CPU
Imax = 0.21A
+1VSUS_ORG
Imax=4.785A

Custom Design
Title: POWER FLOW
<OrgName>
Engineer: <OrgAddPT>
Size: Custom
Project Name: SHIELD
Rev: 1.00
Date: Thursday, August 03, 2017
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15W SOC (CPU SKYLAKE-U)		
+VCORE	-> 29A	
+VCCGT	-> 56A	(GT2e)
	-> 62A	(GT3e)
+VCCSA	-> 5.1A	
+VCCIO	-> 3.1A	
+VCCEDRAM	-> 3A	(GT3e)
+VCCEOPIO	-> 3A	(GT3e)
+VCCST_CPU	-> 0.24A	
+VCCPLL_OC	-> 0.26A	
+DDR_V	-> 2A	
(+1P2V_DUAL)		

(PCH)	
+VCCST	-> 0.04A
+VCCSTG	-> 0.04A
+1V_MODPHY	-> 2.766A
+1VSB	-> 0.782A
+VPCHCORE	-> 3A
+1P8VSB	-> 0.5A
+3P3VSB	-> 0.6A

LPDDR3	
+1P8V_DUAL	-> 0.717A
+1P2V_DUAL	-> 3.5A
+V_VDDQ_VTT (0.6V)	-> 1A

SSD (PCIE/mSATA)	
+3P3V	-> 2.5A

EC	
+3P3V_EC	-> 0.0375A

EC ROM	
+3P3V_EC	-> 0.015A

Temp sensor(STTS751)	
+3P3V_EC	-> 0.0005A (2PCS)

TPM(Infineon SLB9665 ESS2)	
+3P3V_TPM (+3P3V)	-> 0.1A

WiFi&BT	
+3P3V_WWAN	-> 1.5A

DMIC	
DMIC_+3P3V/+3P3V_AUDIO	-> 0.02A

FAN	
+5V_FAN	-> 0.7A

UEFI_SPI_BIOS_ROM	
+3P3V	-> 0.04A

Panel	
VCC_EDP_BKLT_IN	-> 0.12A (30V)
+3P3V_PANEL	-> 1.5A

Touch Interface	
+1P8V_TS	-> 0.452A
+5V_TS	-> 0.22A

ALC298 CODEC	
+5V_AUDIO	-> 1.05A
+1P8V_AUDIO	-> 0.4A

DSP ALC5677	
+1P8V_AUDIO	-> 0.1A

Camera REAR	
+1P2V_CAM_R	-> 0.2A
+1P8V_CAM_R	-> 0.001A
+2P8V_CAM_R	-> 0.048A
+3P3V_VCM	-> 0.125A
+3P3V (LED)	-> 0.005A

Camera FRONT	
+1P8V_CAM_F	-> 0.096A
+2P8V_CAM_F	-> 0.06A
+3P3V (LED)	-> 0.008A

Sensor uC(MKL17Z256VMP4)	
+3P3VA	-> 0.001A

SL1	
+3P3V_HPD	->0.075A

ACT_BOARD	
+3P3VSB	->2A (LEFT+RIGHT)

Hall effect sensor(BU52058GWZ-E2)	
+3P3VA	->0.0028A

Compass(MMC3416XMA)	
+3P3V_SENSOR	->0.0012A

Acceleromte&Gyro(BMI160)	
+3P3V_SENSOR	-> 0.001A

ALS(ISL29033IROZ-T7)	
+3P3V_SENSOR	-> 0.000075A

MUX	
+3P3V_MUX	-> 0.0033A

mini DP	
+3P3V	-> 0.5A

Battery Charger BQ24735	
+6VA_12VA	-> 0.003A

Authentication IC (ECC108)	
+3P3VA	-> 0.005A

<Core Design>

Title: POWER DISTRIBUTION

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	CHARIOT	1.00

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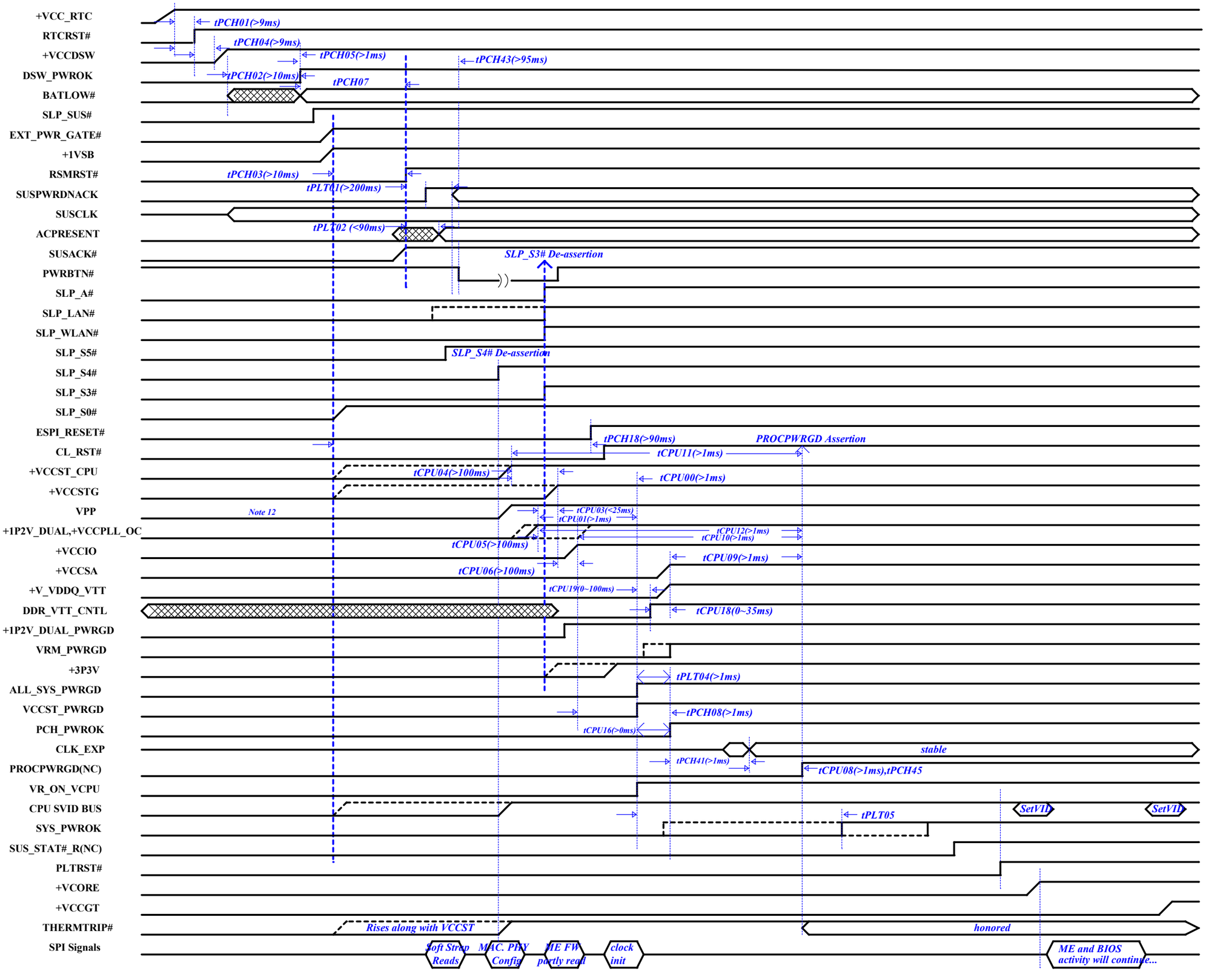
S5 to S0 Power Sequence



<Core Design>

Title:	POWER SEQUENCE	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
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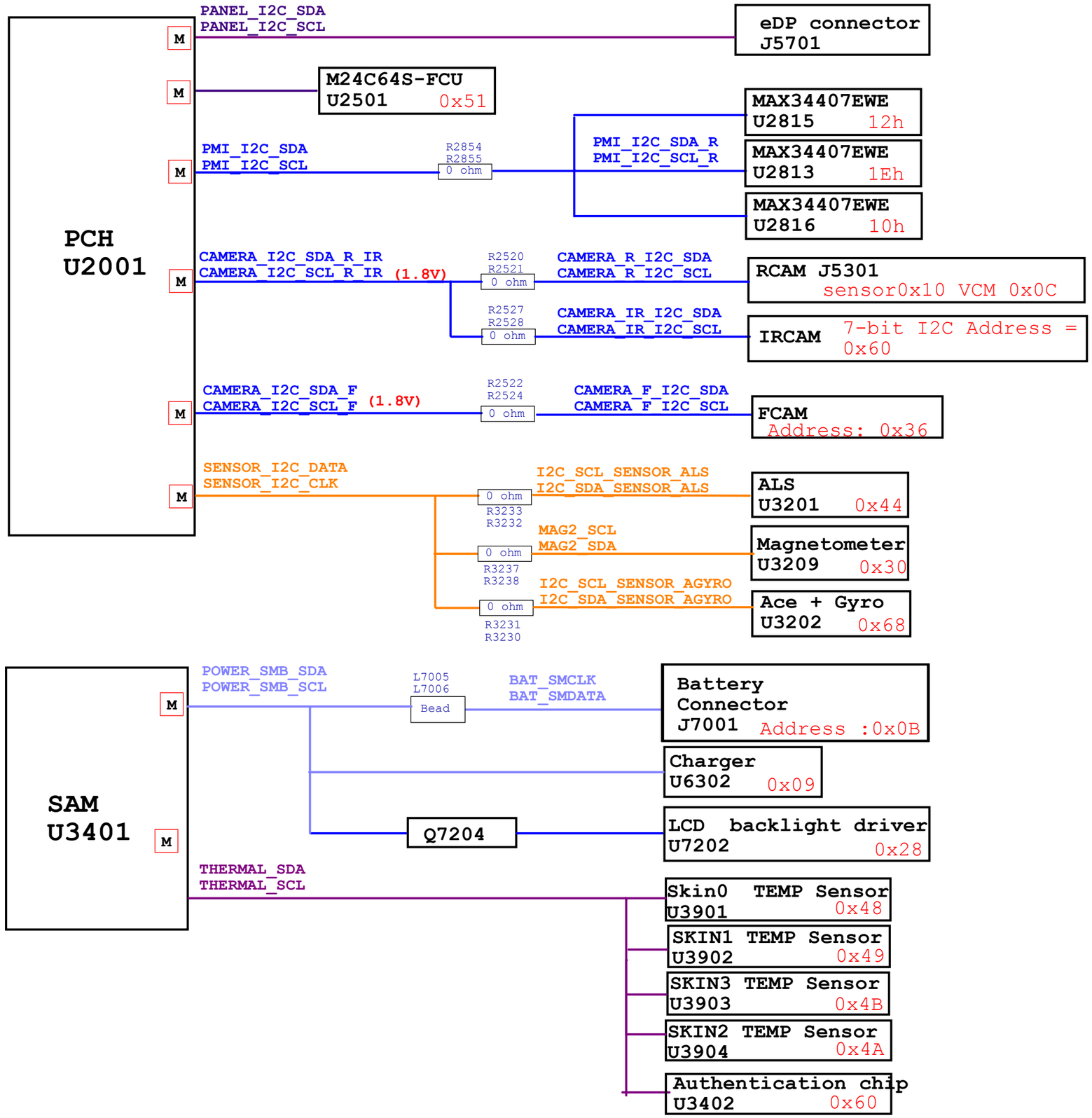
I2C & SMBUS Map



Title:	I2C MAP		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 9 of 76		

TBL1001

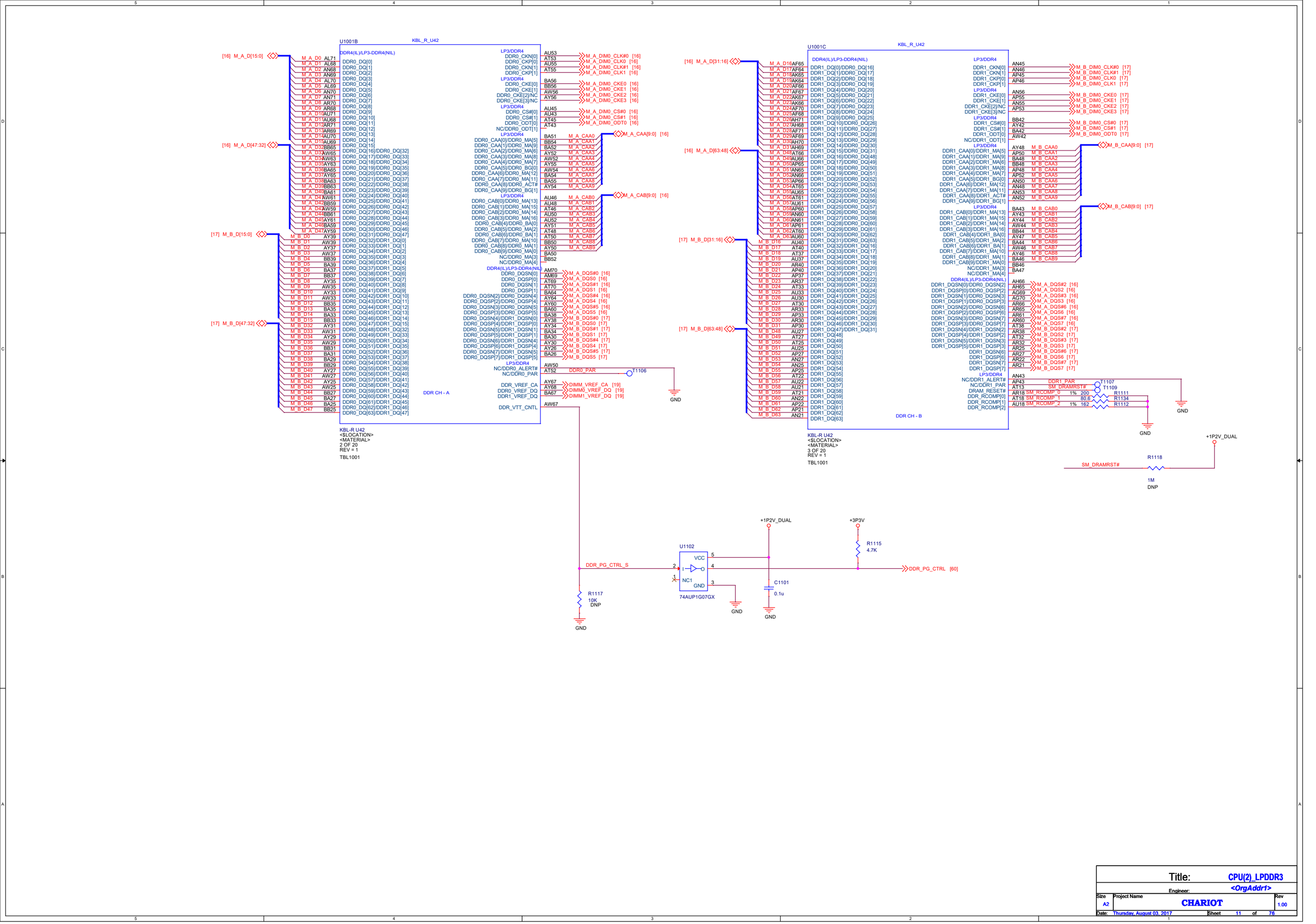
SKU	Proc #	MSPN#
KBL U42 Pre-ES		M1029632-001
KBL U42 ES High-Bin		M1029635-001
KBL U42 ES Low-Bin		M1034578-001
KBL U42 i5 QS		M1029637-001
KBL U42 i7 QS		M1029638-001
KBL U42 i5 PRQ		M1029639-001
KBL U42 i7 PRQ		M1020597-001

DDI Port 1/DDPB: base port (REMOVED)

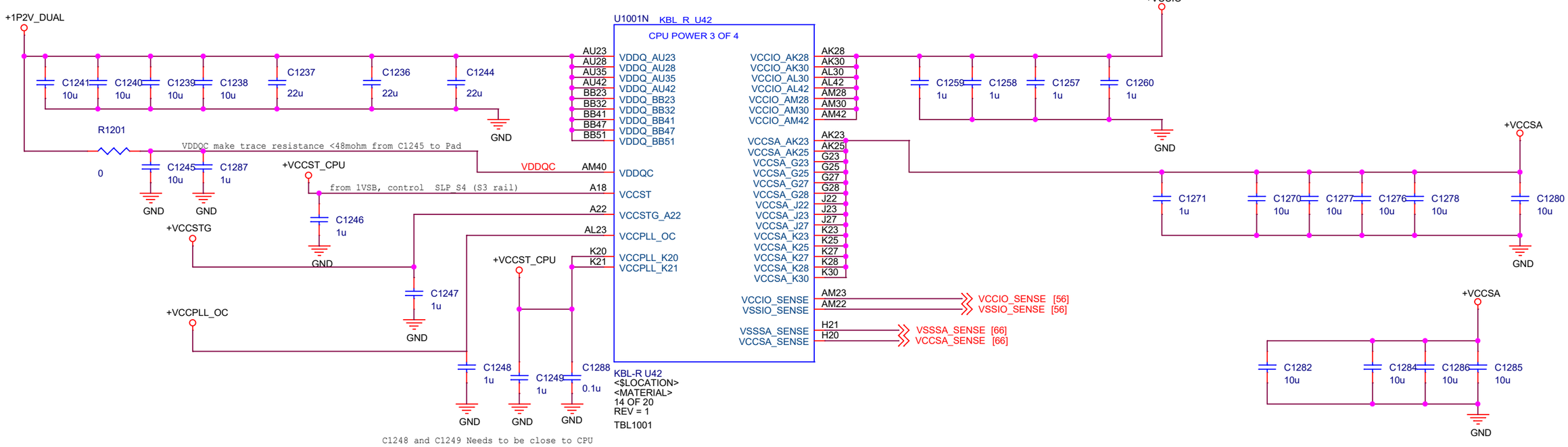
DDI Port 2: SL1

eDP x 4

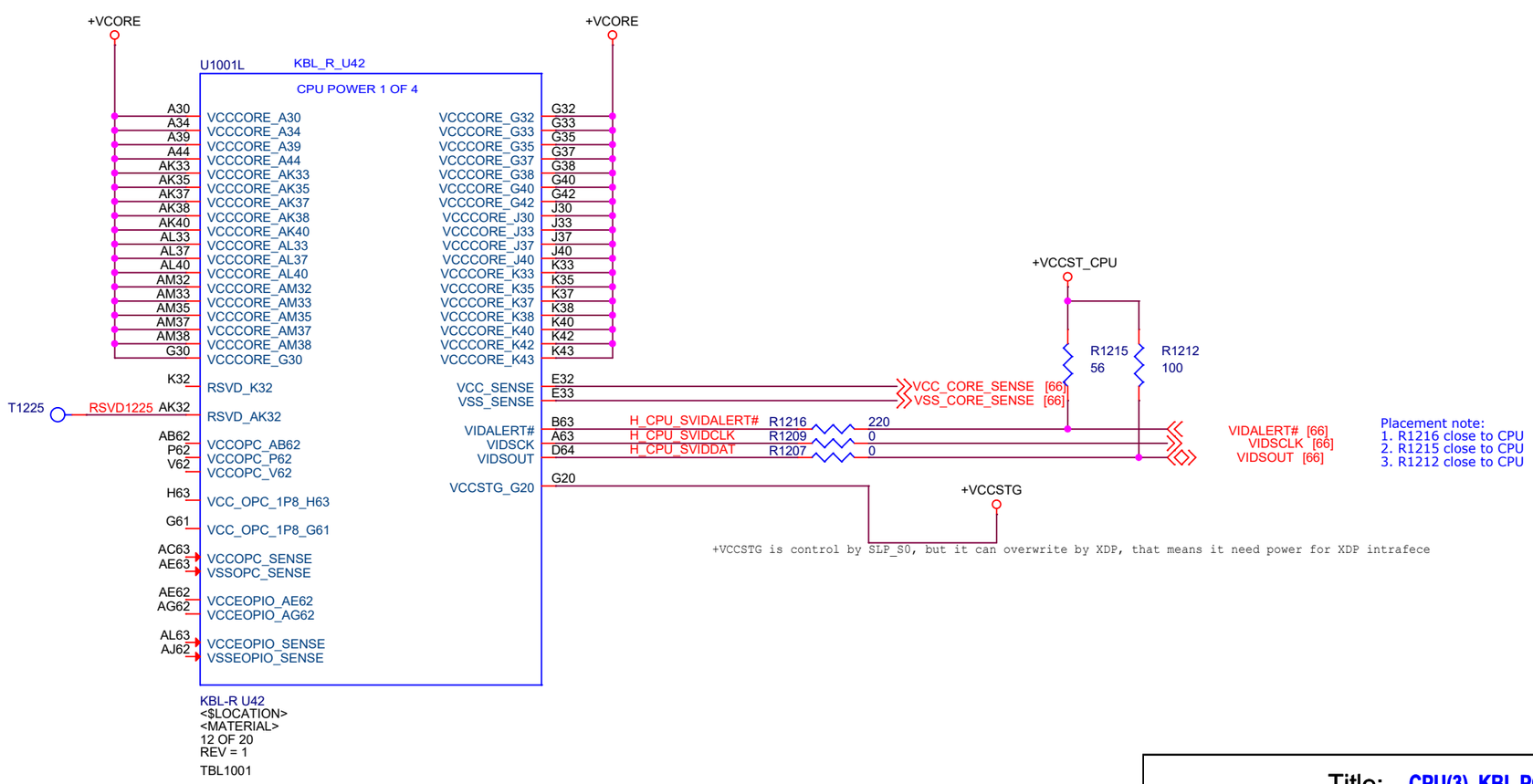
Title: CPU(1)_MISC,JTAG,DDI,EDP		
Engineer: <OrgAddr1>		
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 10 of 76	



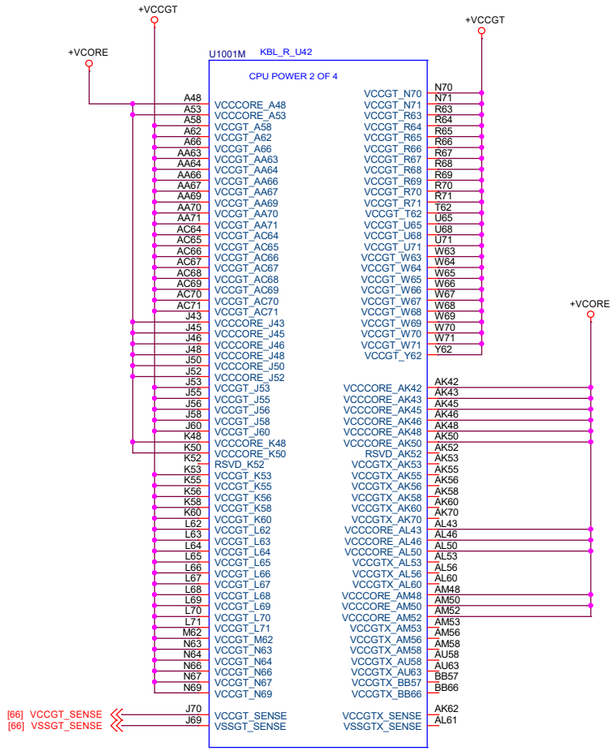
Title:	CPU(2)_LPDDR3		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 11 of 76		

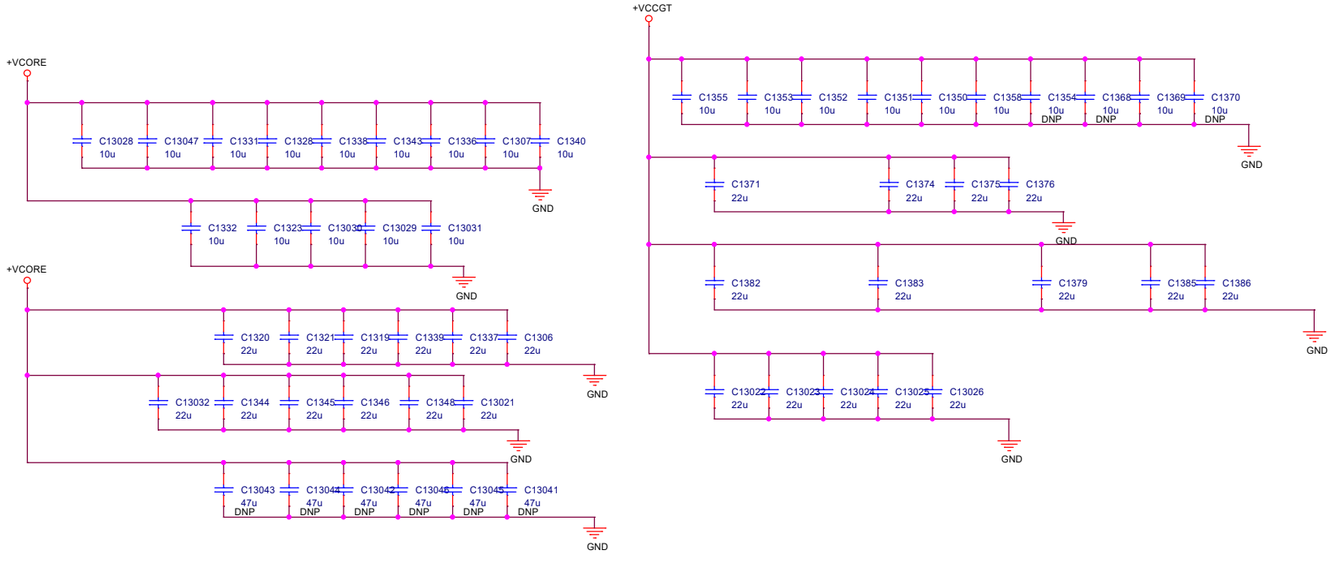


Do not route VccPLL, VccSTG, VccPLL_OC closest adjacent layer over any power net other than ground.

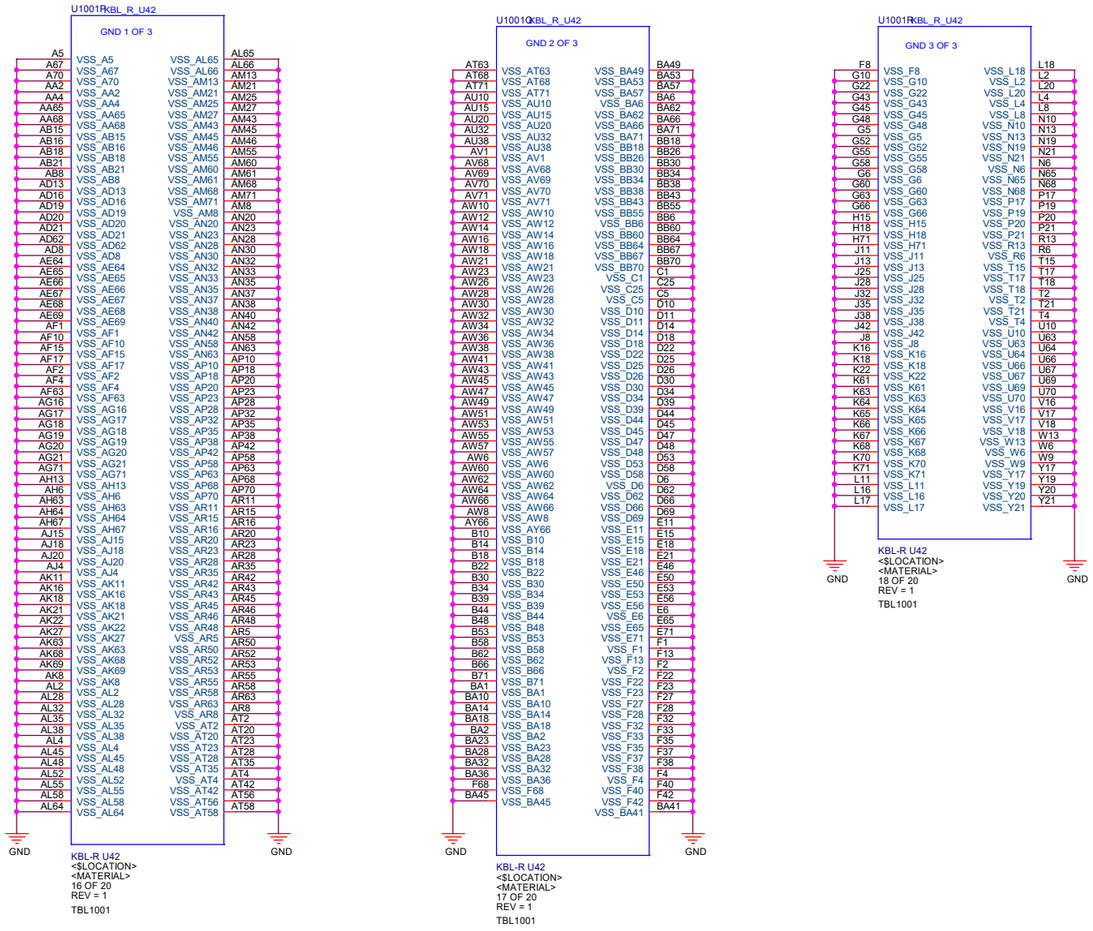


Title:	CPU(3)_KBL POWER1	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 12 of 76	

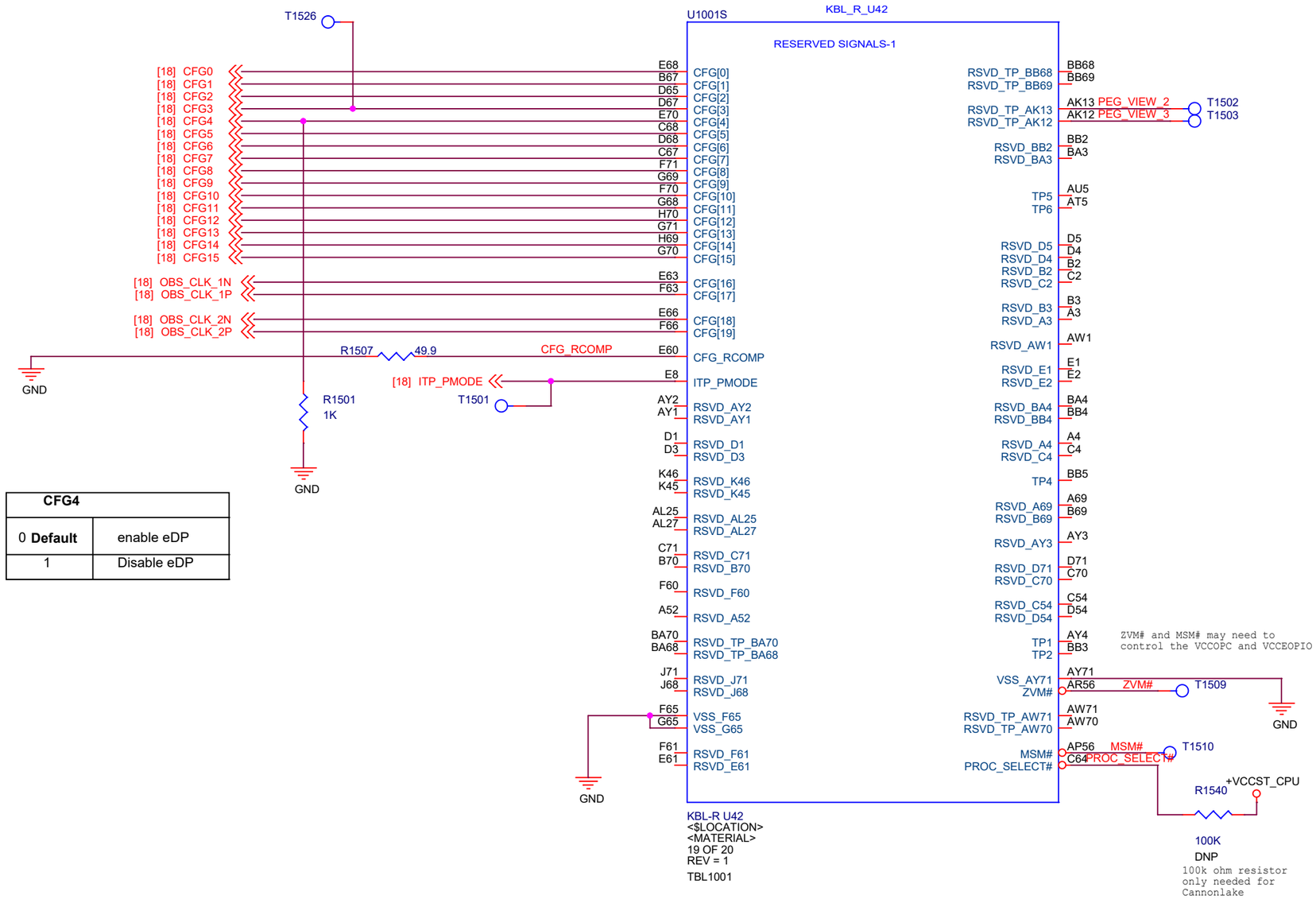




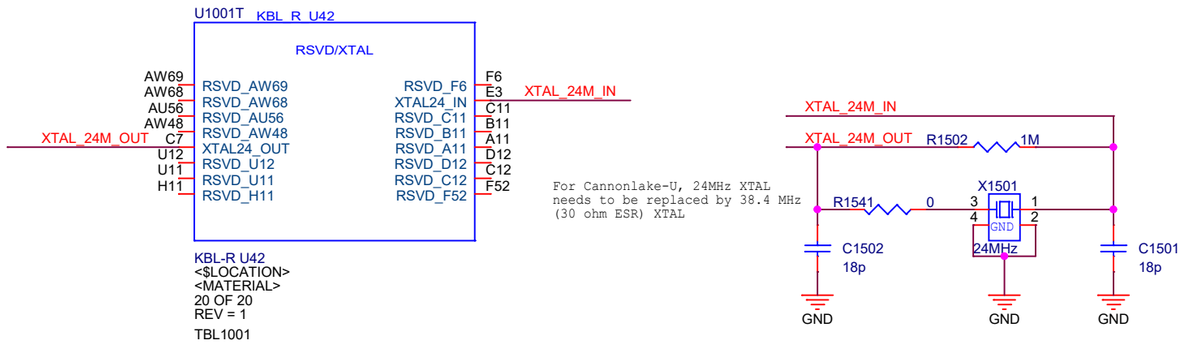
Title:	CPU(4)_KBL_POWER2_GT_VCORE		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 13 of 76		



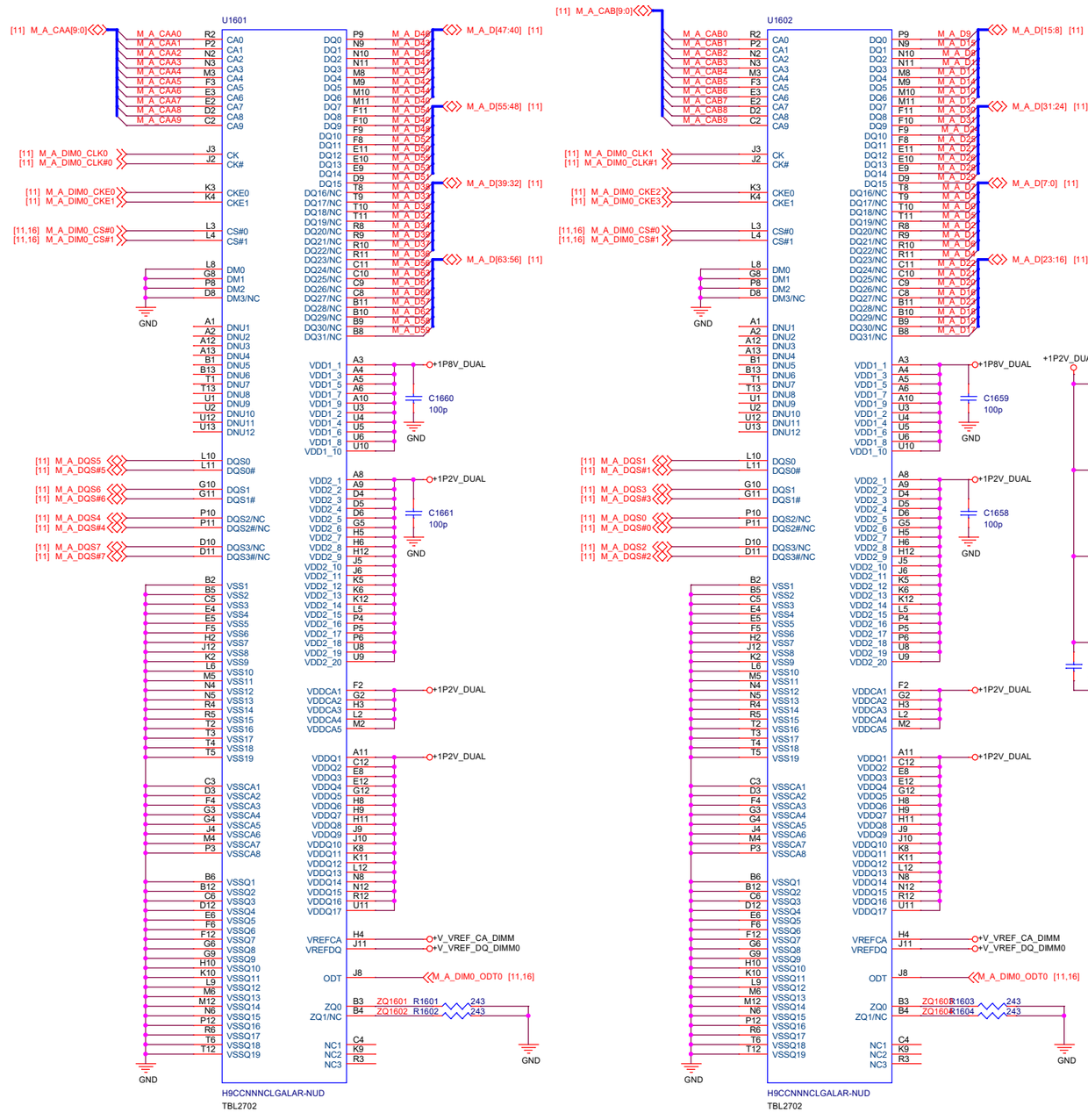
Title:	CPU(5)_GND		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 14 of 76		



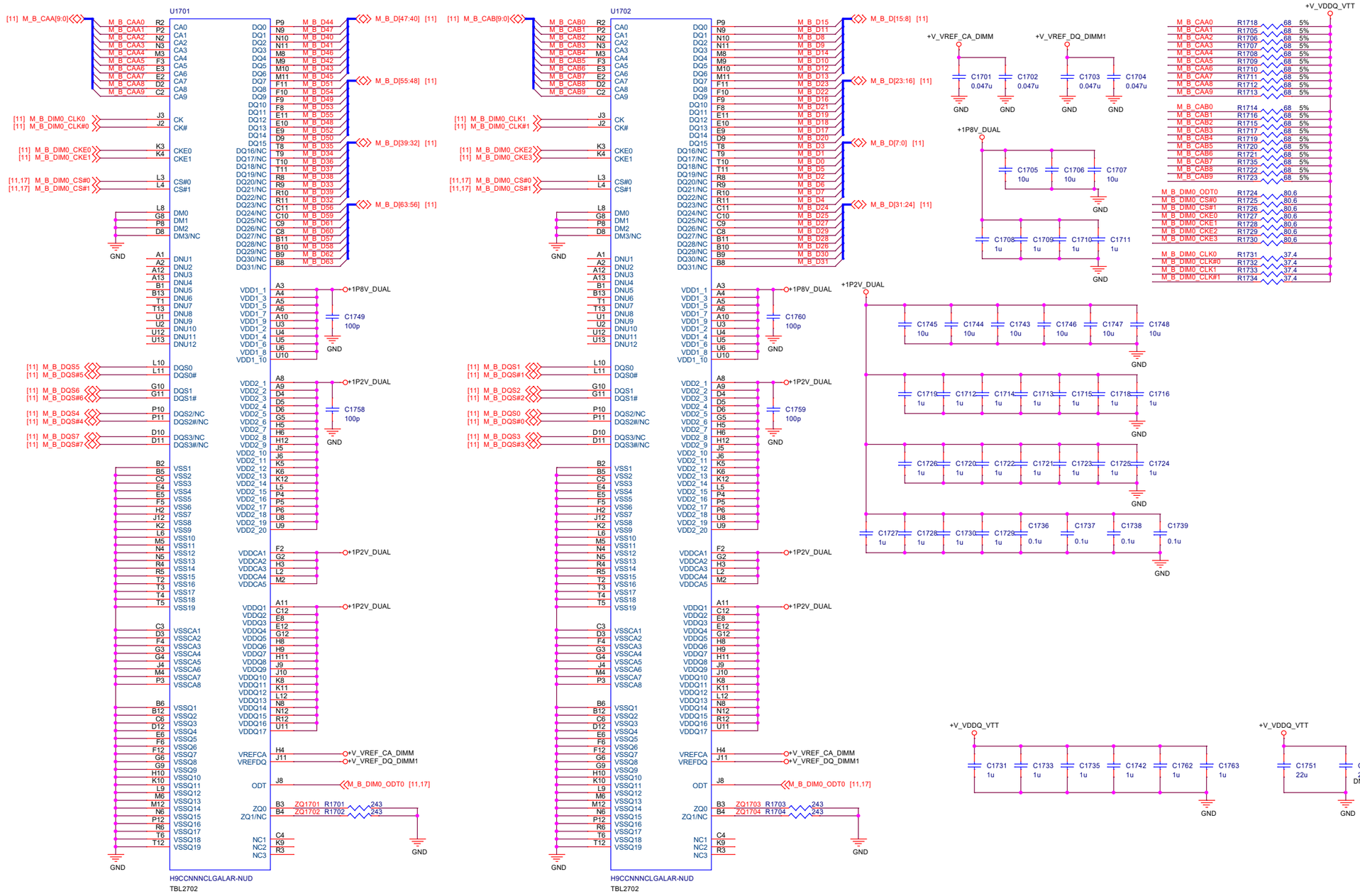
CFG4	
0 **Default**	enable eDP
1	Disable eDP



Title: CPU(6)_CFG_RESERVED			
Engineer: <OrgAddr1>			
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 15 of 76		

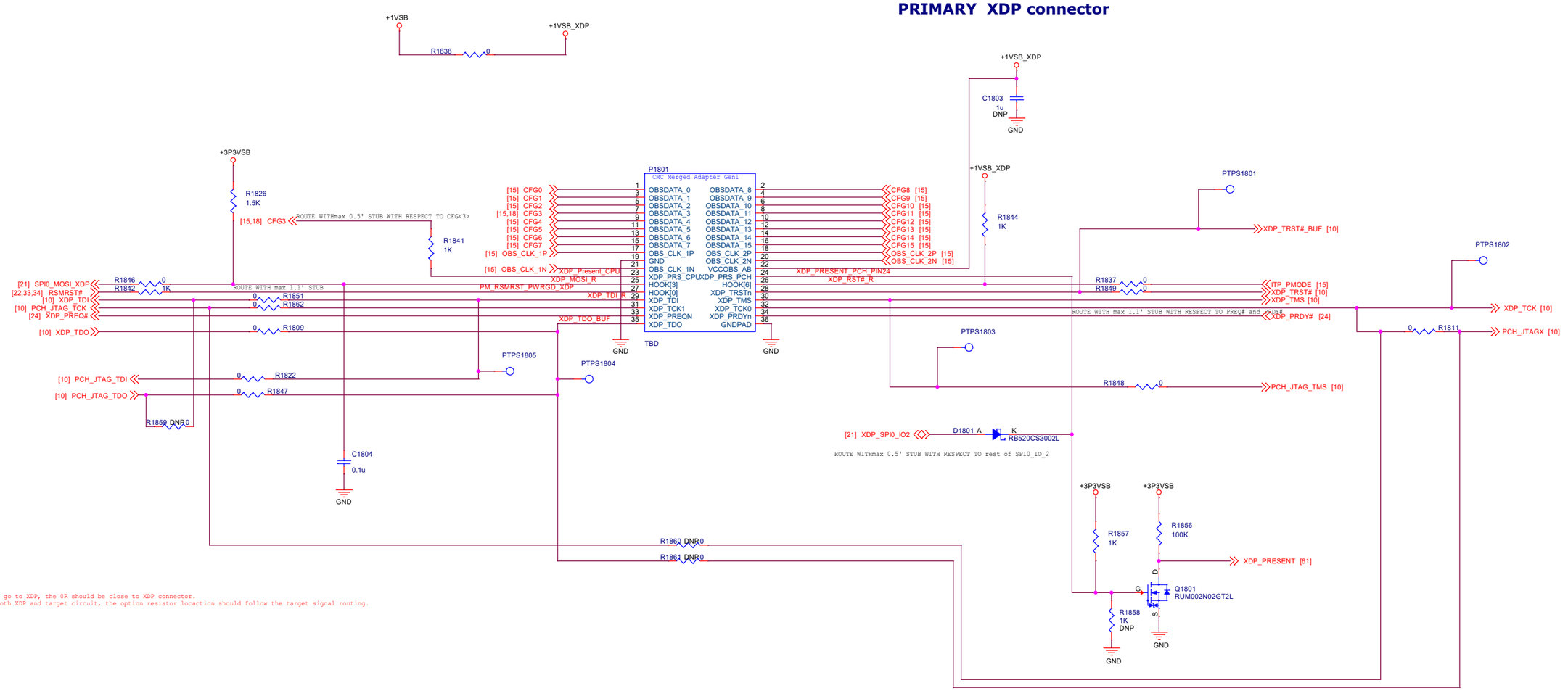


Title: LPDDR3(1)_MEMORY DOWN			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 16 of 76		



Title: LPDDR3(2)_MEMORY DOWN			
Engineer: <OrgAddr1>			
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 17 of 76		

PRIMARY XDP connector



If the signals only go to XDP, the 0R should be close to XDP connector.
If the signals to both XDP and target circuit, the option resistor locaction should follow the target signal routing.

OBS_CLK Routing

Stub length: 200ps (approx. 1100mil or 28mm). The stub length should be minimized whenever possible.

Trace-to-Trace spacing: 3 x Trace Width

Maximum Via count: 4

Maximum Trace length: 2ns (roughly 12000mil or 305mm)

Length Matching: within +/- 270mil (6.85mm) of CFG[17]

CFG Routing

Termination: None

Stub length: 200ps (approx. 1100mil or 28mm). The stub length should be minimized whenever possible.

Trace-to-Trace spacing: No limit, but 2x trace width when possible

Maximum Via count: No limit, but should minimize whenever possible

Maximum Trace length: 2ns (roughly 12000mil or 305mm) (For each segment, measures from XDP OBS pin ->Skylake pin)

Length Matching: within +/- 270mil (6.85mm) of CFG[17]

Title: XDP			
Engineer: <OrgAddr1>			
Size: A2	Project Name: CHARIOT		Rev: 1.00
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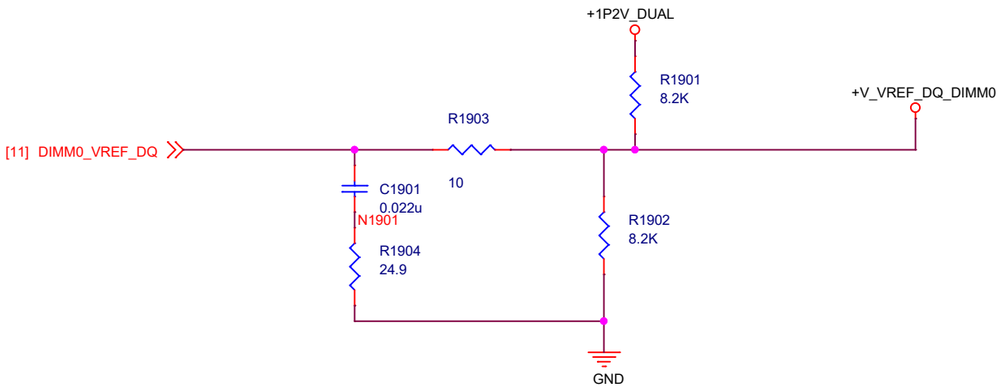
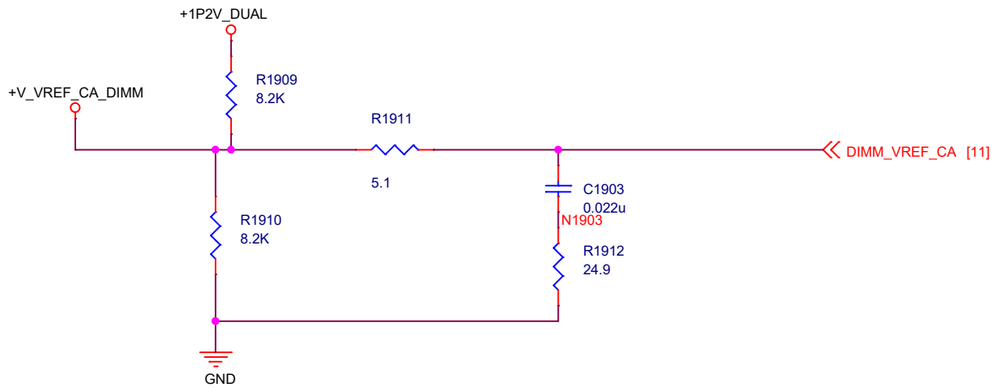
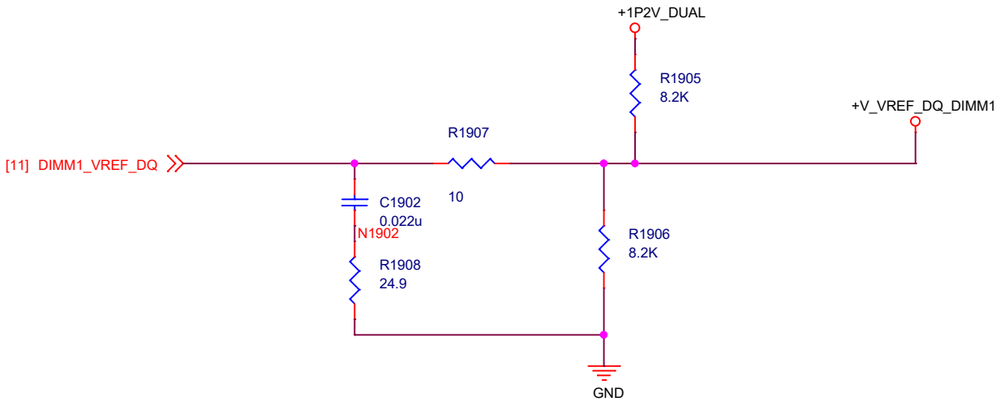
LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off







Title: LPDDR3(3)_CA/DQ Voltage		
Engineer: *<OrgAddr1>*		
Size: A3	Project Name: **CHARIOT**	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 19 of 76	

PCIE_CLK_0	
PCIE_CLK_1	SSD
PCIE_CLK_2	
PCIE_CLK_3	SL1
PCIE_CLK_4	PGU
PCIE_CLK_5	WIFI

+3P3V

R2052 10K
R2050 10K
R2048 10K

[43] PCIE_SSD_PERST# — 0 DNP R2011 — PCIE_SSD_PERST#_R

[43] PCIECLK_SSD_N
[43] PCIECLK_SSD_P

[33,43] SSD_PCIECLK_REQ_N

[65] ACC_PWR_EN

[73] PCIE_GPU_RCLK_N
[73] PCIE_GPU_RCLK_P

[73] PCIE_GPU_CLKREQ_N

[50] PCIE_WIFI_RCLK_N
[50] PCIE_WIFI_RCLK_P

[33,50] PCIE_WIFI_CLKREQ_N

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CLOCK SIGNALS

D42	CLKOUT_PCIE_N0	
C42	CLKOUT_PCIE_P0	
AR10	GPP_B5/SRCCLKREQ0#	PCIE_SSD_PERST#_R
B42	CLKOUT_PCIE_N1	[43] PCIECLK_SSD_N
A42	CLKOUT_PCIE_P1	[43] PCIECLK_SSD_P
AT7	GPP_B6/SRCCLKREQ1#	[33,43] SSD_PCIECLK_REQ_N
D41	CLKOUT_PCIE_N2	
C41	CLKOUT_PCIE_P2	
AT8	GPP_B7/SRCCLKREQ2#	[65] ACC_PWR_EN
D40	CLKOUT_PCIE_N3	
C40	CLKOUT_PCIE_P3	
AT10	GPP_B8/SRCCLKREQ3#	
B40	CLKOUT_PCIE_N4	[73] PCIE_GPU_RCLK_N
A40	CLKOUT_PCIE_P4	[73] PCIE_GPU_RCLK_P
AU8	GPP_B9/SRCCLKREQ4#	[73] PCIE_GPU_CLKREQ_N
E40	CLKOUT_PCIE_N5	[50] PCIE_WIFI_RCLK_N
E38	CLKOUT_PCIE_P5	[50] PCIE_WIFI_RCLK_P
AU7	GPP_B10/SRCCLKREQ5#	[33,50] PCIE_WIFI_CLKREQ_N

CLKOUT_ITPXDP_N	F43	CLK_XDP_N — T2009
CLKOUT_ITPXDP_P	E43	CLK_XDP_P — T2010
GPD8/SUSCLK	BA17	SUSCLK — T2008
NC_2	E37	
NC_1	E35	
XCLK_BIASREF	E42	XCLK_BIASREF
RTCX1	AM18	RTC_X1
RTCX2	AM20	RTC_X2
SRTCRST#	AN18	SRTC_RST# — T2002
RTCRST#	AM16	T2007

[35] RTC_RST#

E42 Pulled to ground for Cannonlake-U support via 60 ohm (+/-1%) resistor. Intel confirms 60.4 ohm is fine Dec1

VCCCLK5_R

R2036 2.7K
R2090 60.4 DNP
GND

R2001 10M

R2005 0
X2001 CTAL_1 1 2 32.768MHz
C2001 18p
C2002 18p
GND GND

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+VCC_RTC

R2021 20K — SRTC_RST# — C2003 1u — GND

R2002 20K — RTC_RST# — C2004 1u — GND

HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.HDA_SDOwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

+1P8VSB
R2009 DNP 1K

U1001G KBL_R_U42

AUDIO

[40] AZ_SYNC_1	R2020 33	HDA_SYNC_R — BA22 HDA_SYNC/I2S0_SFRM
[40] AZ_BITCLK_1	R2053 33	HDA_BCLK_R — AY22 HDA_BLK/I2S0_SCLK
[40] AZ_SDATA_OUT_1	R2054 33	HDA_SDO_R — INT. PD — BB22 HDA_SDO/I2S0_TXD
[40] AZ_SDATA_IN0		BA21 HDA_SDI0/I2S0_RXD
	T2004	HDA_SDI1_DSP — AY21 HDA_SDI1/I2S1_RXD
		HDA_RST# — AW22 HDA_RST#/I2S1_SCLK
		J5 GPP_D23/I2S_MCLK
	T2003 T2005	I2S1SFRM — AY20 I2S1_SFRM
		I2S1_TXD — AW20 I2S1_TXD
		AK7 GPP_F1/I2S2_SFRM
		AK6 GPP_F0/I2S2_SCLK
		AK9 GPP_F2/I2S2_TXD
		AK10 GPP_F3/I2S2_RXD
		H5 GPP_D19/DMIC_CLK0
		D7 GPP_D20/DMIC_DATA0
		D8 GPP_D17/DMIC_CLK1
		C8 GPP_D18/DMIC_DATA1
		AW5 GPP_B14/SPKR

C2009 2p GND
C2010 2p GND
C2008 2p GND

+3P3VA
C2005 0.1u GND

+3P3V
R2006 1K

U2001 SN74LVC2G66YZPR
VCC A2
1A A1 — TOP_SWAP_1A
1EN B2
2A D2
2EN C1
2B C2 — TOP_SWAP
GND D1
1B B1

[35] UEFI_TOP_SWAP
R2004 100K GND

INT. PD
R2007 47K GND

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SDIO/SDXC

GPP_G0/SD_CMD	AB11	TS_BRD_REV[0] [30]
GPP_G1/SD_DATA0	AB13	TS_BRD_REV[1] [30]
GPP_G2/SD_DATA1	AB12	TCON_VENDOR_ID [57]
GPP_G3/SD_DATA2	W12	
GPP_G4/SD_DATA3	W11	CH_A_N
GPP_G5/SD_CD#	W10	CH_B_N
GPP_G6/SD_CLK	W8	
GPP_G7/SD_WP	W7	
GPP_A17/SD_PWR_EN#/ISH_GP7	BA9	CAM_LED_R_EN [53]
GPP_A16/SD_1P8_SEL	BB9	WLAN_PWD_N [33,50]
SD_RCOMP	AB7	SD_RCOMP
GPP_F23	AF13	

R2080 200 GND

+3P3VSB +3P3VSB
R2096 10K DNP
R2098 10K DNP
R2097 10K
R2095 10K
GND GND GND

+3P3V

R2093	47K	TCON_VENDOR_ID
R2094	47K	TS_BRD_REV[0]
R2091	47K	TS_BRD_REV[1]
R2010 DNP	47K	PCIE_SSD_PERST#
R2056	47K	WLAN_PWD_N
R2055	47K	ACC_PWR_EN

GND

Enable LPDDR3 memory channel for debug purpose

	CH_A_N	CH_B_N
A and B ON	0	0
only B ON	1	0
only A ON	0	1

STP_A16OVR:

A16 swap override Strap/ Top-Block swap override jumper

High=Enabled A16 swap override/ Top-Block swap override
Low=Default

Title: PCH(1)_SD,HDA,RTC,CLK

Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	CHARIOT	1.00

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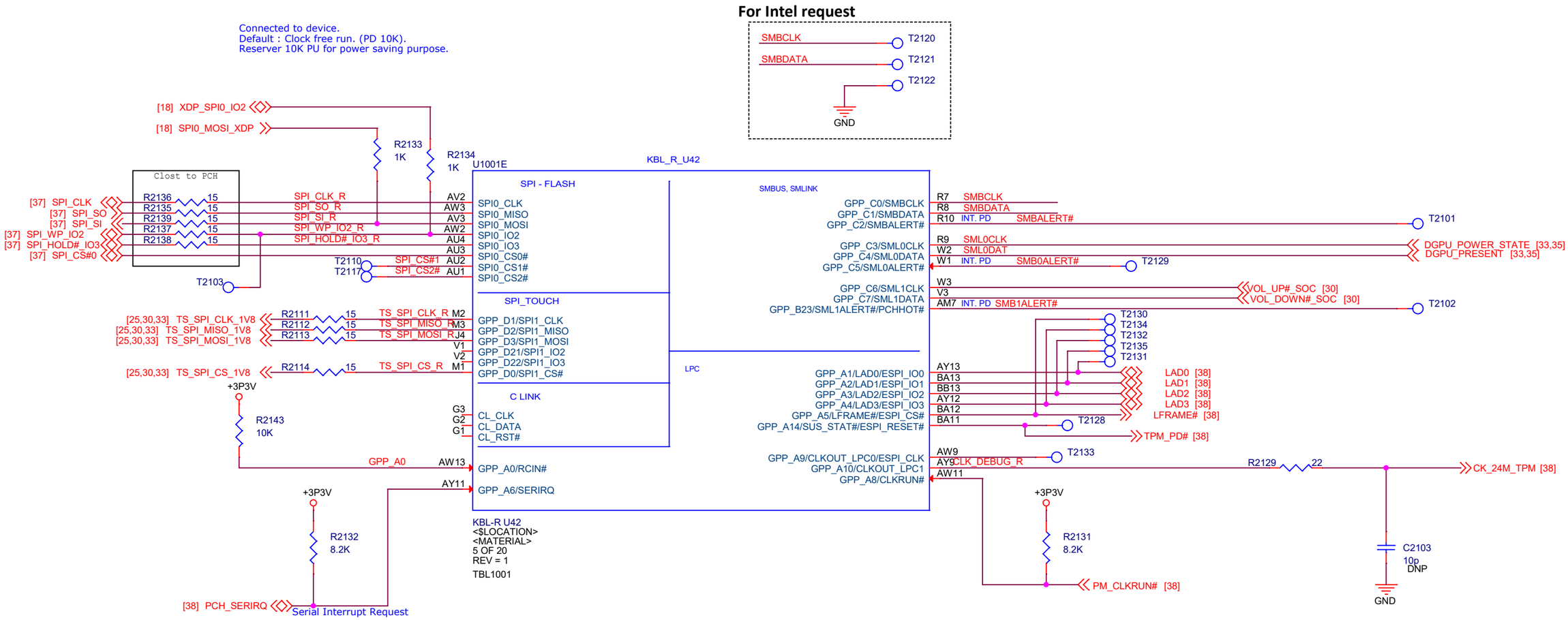
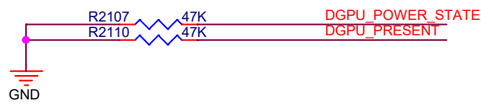
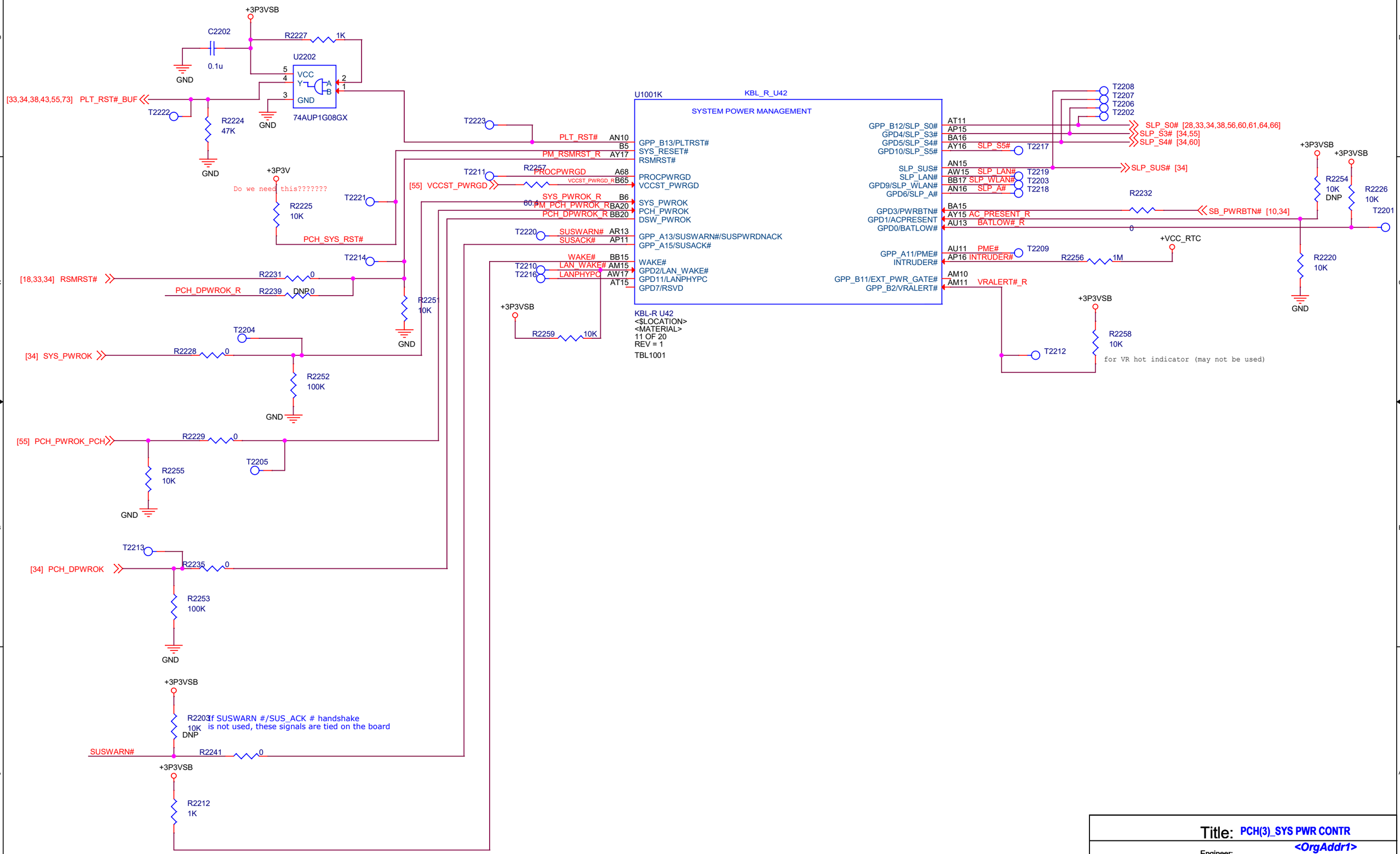


GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SML0ALERT#	
0 **Default**	LPC **(EC)**
1	eSPI **(EC)**



Title:	PCH(2)_CLK,SMB,LPC,SPI		
Engineer:	<OrgAddr1>		
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017		Sheet 21 of 76	



Title:	PCH(3)_SYS PWR CONTR		
Engineer:	<OrgAddr1>		
Size: A3	Project Name: CHARIOT		Rev: 1.00
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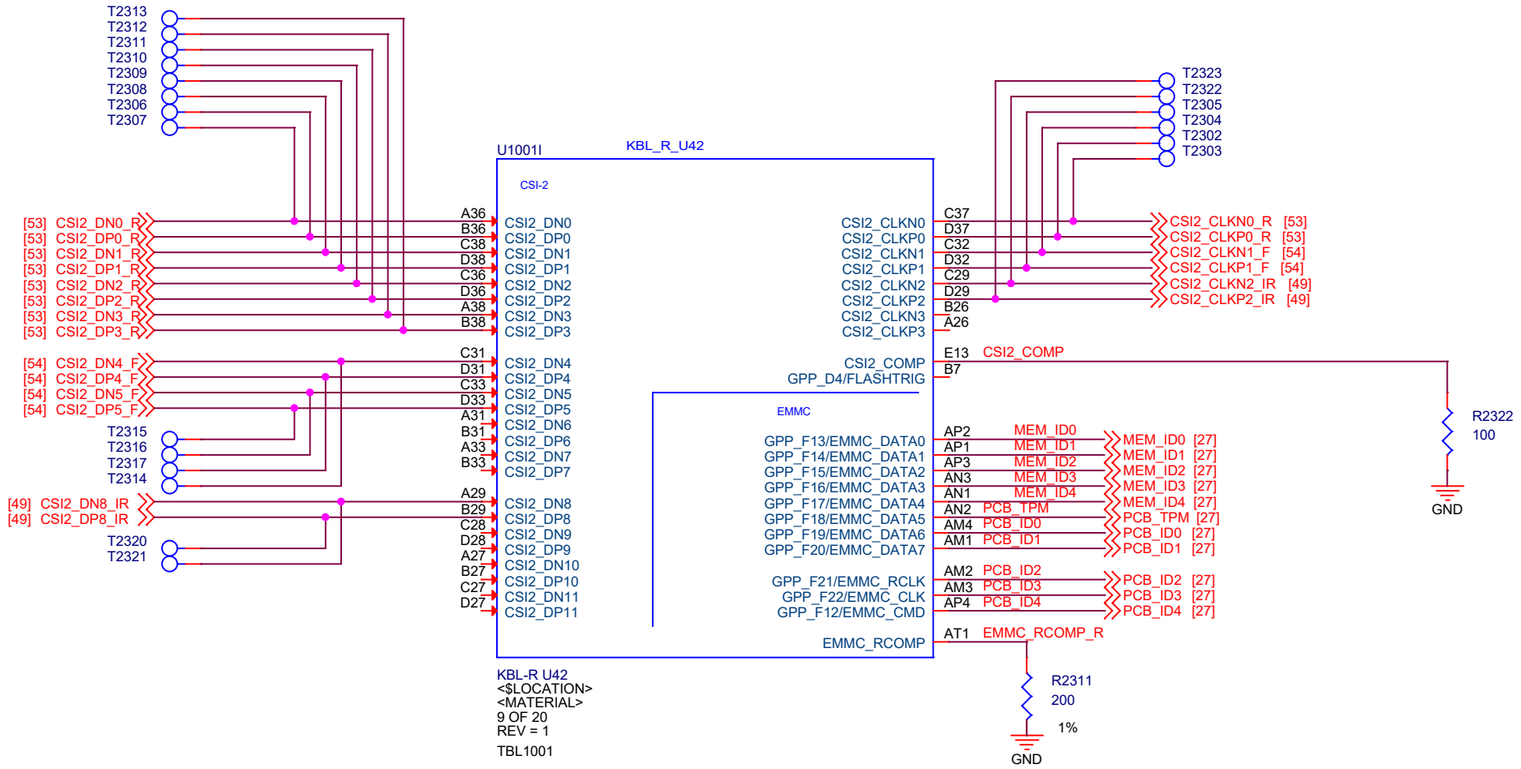
Those test point will be removed after check CSI



Title:	PCH(4)_CCI, HWID	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
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PCIE/USB3/SATA

SSIC / USB3

USB2

PCIE WIFI

[50] PCIE_WIFI_RXN1
[50] PCIE_WIFI_RXP1
[50] PCIE_WIFI_TXN1
[50] PCIE_WIFI_TXP1

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

PCIE GPU

[71,73] PCIE_GPU_RN5_L0
[71,73] PCIE_GPU_RP5_L0
[73] PCIE_GPU_TN5_L0
[73] PCIE_GPU_TP5_L0

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

[71,73] PCIE_GPU_RN5_L1
[71,73] PCIE_GPU_RP5_L1
[73] PCIE_GPU_TN5_L1
[73] PCIE_GPU_TP5_L1

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

[71,73] PCIE_GPU_RN5_L2
[71,73] PCIE_GPU_RP5_L2
[73] PCIE_GPU_TN5_L2
[73] PCIE_GPU_TP5_L2

F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

[71,73] PCIE_GPU_RN5_L3
[71,73] PCIE_GPU_RP5_L3
[73] PCIE_GPU_TN5_L3
[73] PCIE_GPU_TP5_L3

G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

[43] PCIE_SSD_RN0
[43] PCIE_SSD_RP0
[43] PCIE_SSD_TN0
[43] PCIE_SSD_TP0

E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

[43] PCIE_SSD_RN1
[43] PCIE_SSD_RP1
[43] PCIE_SSD_TN1
[43] PCIE_SSD_TP1

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

+3P3V
R2328 10K

PCIE_RCOMPN F5
R2401 100 1% PCIE_RCOMPP E5
PCIE_RCOMP_N
PCIE_RCOMP_P

T2417
[18] XDP_PRDY# D56
PROC_PRDY#
[18] XDP_PREQ# D61
PROC_PREQ#
T2418
T2419 PIRQA# BB11
GPP_A7/PIRQA#

SSD GPU

[43] PCIE_SSD_RN2
[43] PCIE_SSD_RP2
[43] PCIE_SSD_TN2
[43] PCIE_SSD_TP2
[43] PCIE_SSD_RN3
[43] PCIE_SSD_RP3
[43] PCIE_SSD_TN3
[43] PCIE_SSD_TP3

E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

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USB3_1_RXN H8
USB3_1_RXP G8
USB3_1_TXN C13
USB3_1_TXP D13

[45] USB3_CONN_RXN1
[45] USB3_CONN_RXP1
[45] USB3_CONN_TXN1
[45] USB3_CONN_TXP1

USB3.0 T to B

USB3_2_RXN/SSIC_RXN J6
USB3_2_RXP/SSIC_RXP H6
USB3_2_TXN/SSIC_TXN B13
USB3_2_TXP/SSIC_TXP A13

USB3_3_RXN J10 USB3_3_RXN
USB3_3_RXP H10 USB3_3_RXP
USB3_3_TXN B15 USB3_3_TXN C2402 0.1u
USB3_3_TXP A15 USB3_3_TXP C2401 0.1u

[33] USB3_A_RX_DEBUG_IN_N
[33] USB3_A_RX_DEBUG_IN_P
[33] USB3_A_TX_DEBUG_OUT_N
[33] USB3_A_TX_DEBUG_OUT_P

For Software DCI checking

USB3_4_RXN E10
USB3_4_RXP F10
USB3_4_TXN C15
USB3_4_TXP D15

[71] USB3_SL1_RXN4
[71] USB3_SL1_RXP4
[71] USB3_SL1_TXN4
[71] USB3_SL1_TXP4

USB3.0 SL1

USB2N_1 AB9
USB2P_1 AB10

[45] USB2_CONN_D-
[45] USB2_CONN_D+

USB T to B

USB2N_2 AD6
USB2P_2 AD7

USB2N_3 AH3
USB2P_3 AJ3

[33] USB2_DEBUG_DM
[33] USB2_DEBUG_DP

USB2N_4 AD9
USB2P_4 AD10

[71] USB2_SL1_D-
[71] USB2_SL1_D+

SL1

USB2N_5 AJ1
USB2P_5 AJ2

USB2N_6 AF6
USB2P_6 AF7

[50] BT_USB_DN
[50] BT_USB_DP

BT

USB2N_7 AH1
USB2P_7 AH2

[48] USB2_XC_D-
[48] USB2_XC_D+

ACC radio

USB2N_8 AF8
USB2P_8 AF9

USB2N_9 AG1
USB2P_9 AG2

USB2N_10 AH7
USB2P_10 AH8

USB2_COMP AB6 USB2_COMP R2402 113 GND
USB2_ID AG3
USB2_VBUSSENSE AG4 GND

GPP_E9/USB2_OC0# A9
GPP_E10/USB2_OC1# C9
GPP_E11/USB2_OC2# D9
GPP_E12/USB2_OC3# B9

GPP_E4/DEVSLP0 J1
GPP_E5/DEVSLP1 J2
GPP_E6/DEVSLP2 J3

GPP_E0/SATAXPCIE0/SATAGP0 H2
GPP_E1/SATAXPCIE1/SATAGP1 H3
GPP_E2/SATAXPCIE2/SATAGP2 G4

GPP_E8/SATALED# H1

Title:	PCH(5)_PCIE,USB	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
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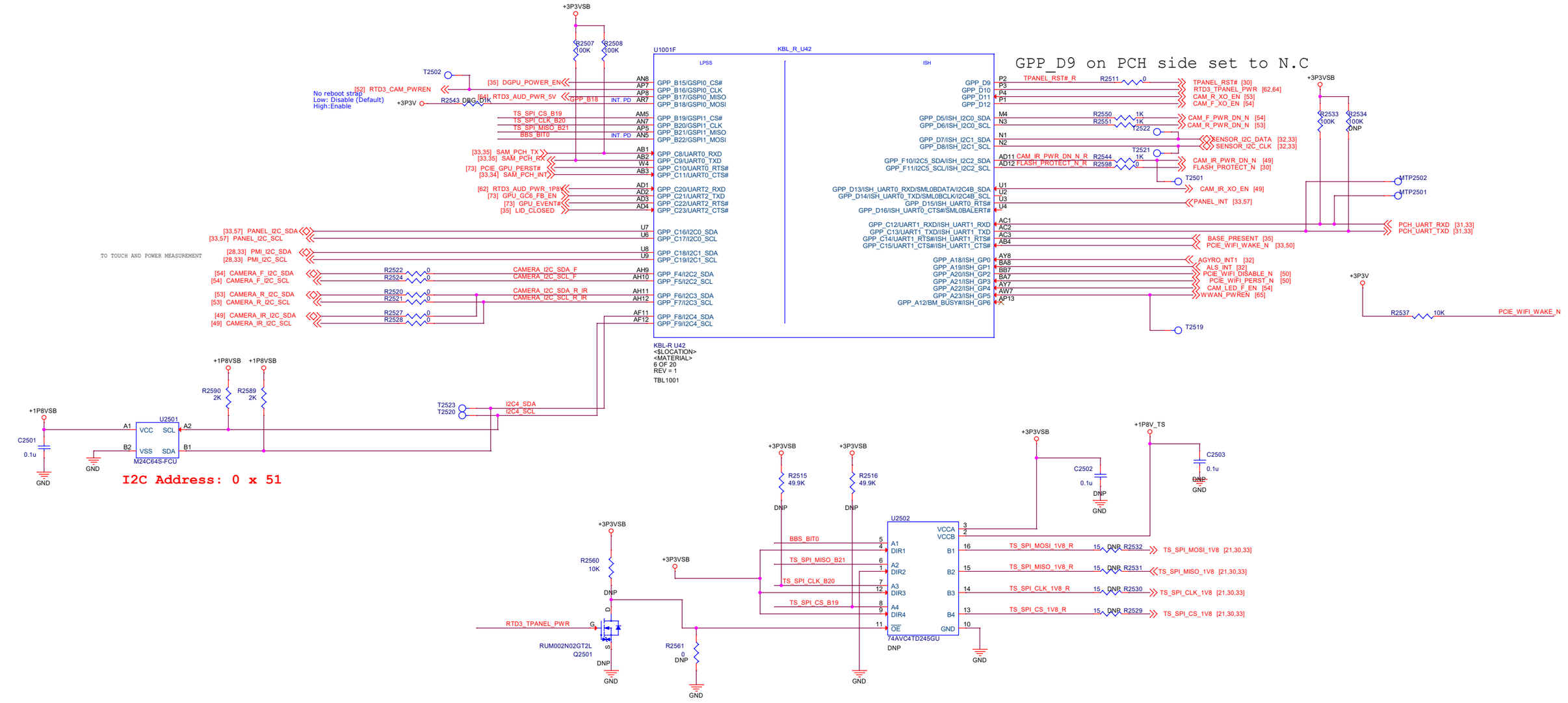
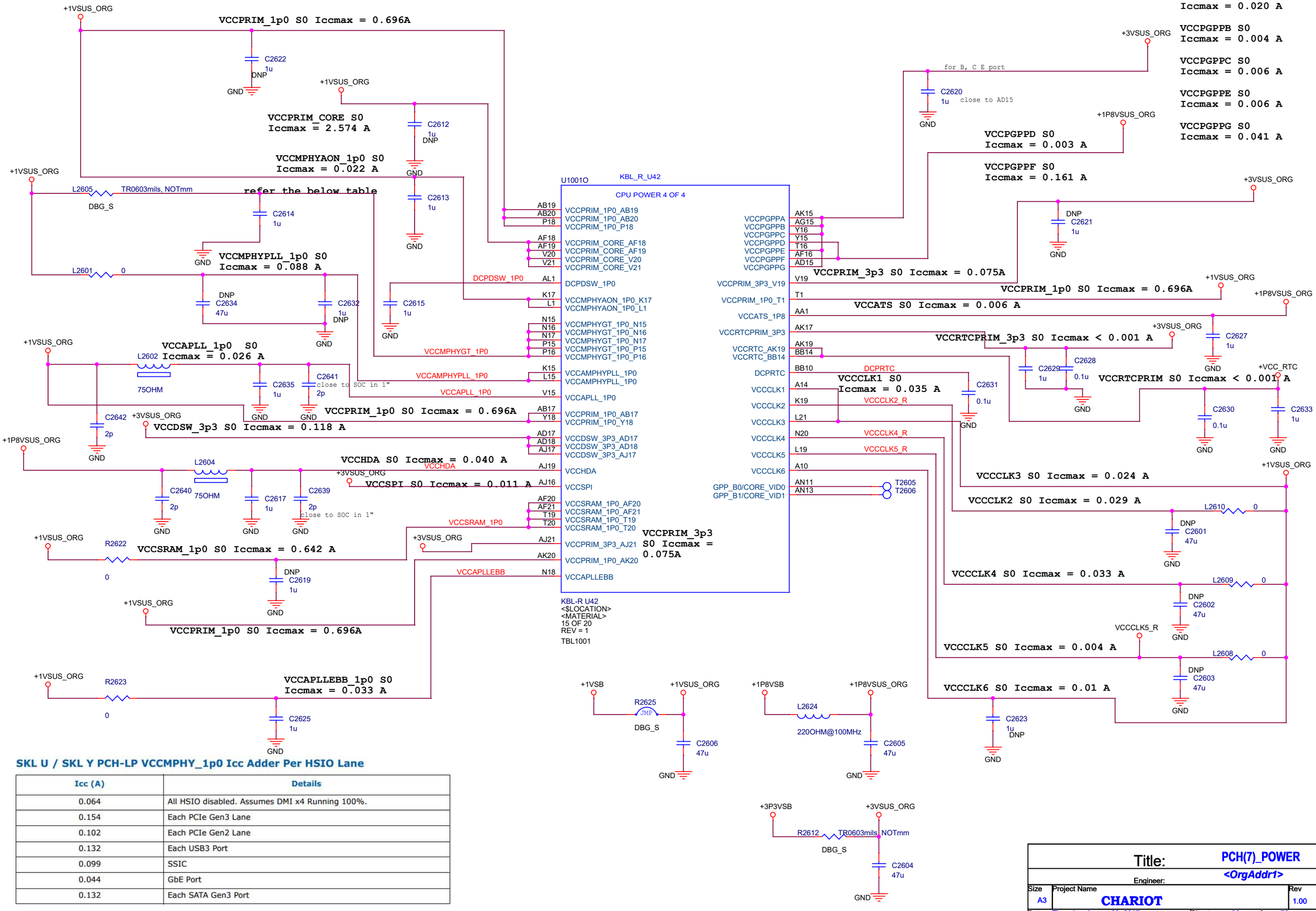


Title:	PCH(6)_CPU,GPIO,MISC	
	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 25 of 76	

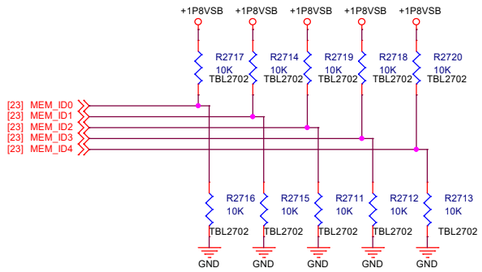


SKL U / SKL Y PCH-LP VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled. Assumes DMI x4 Running 100%.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

Title:	PCH(7)_POWER		
Engineer:	<OrgAddr1>		
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 26 of 76		

	MEM_ID4
1600 LPDDR3	0
1866 LPDDR3	1



	MEM_ID1	MEM_ID0
Hynix 2znm	0	0
Samsung 20nm	0	1

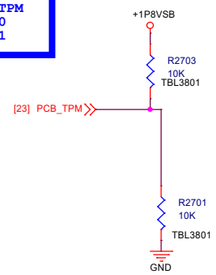
32Gb * 4(pcs) = 16GB
16Gb * 4(pcs) = 8GB
8Gb * 4(pcs) = 4GB

	MEM_ID2	MEM_ID3
4GB	0	0
8GB	1	0
16GB	0	1

	PCBID4	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0
EV3A	1	0	0	1	1
EV3B	1	0	1	1	0
DV	1	0	1	1	1
PV	1	1	0	0	0

	PCB_ID4
Gauntlet	0
Shield	1

	PCB_TPM
Nuvoton / Infineon	0
Nation Z	1

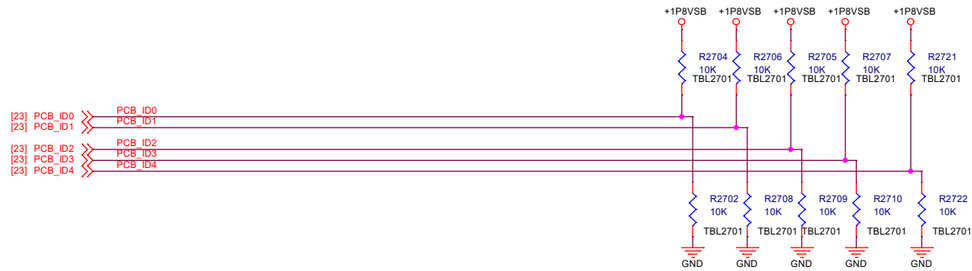


TBL2701

Build	X861217-001 Qty (10K 0201)	PCH_Value	PCH_10K	PCH_NOSTUFF
EV3A	5	10011	R2721, R2710, R2709, R2706, R2704	R2722, R2707, R2705, R2708, R2702
	5	10100	R2721, R2710, R2705, R2708, R2702	R2722, R2707, R2709, R2706, R2704
	5	10101	R2721, R2710, R2705, R2708, R2704	R2722, R2707, R2709, R2706, R2702
EV3B	5	10110	R2721, R2710, R2705,R2706, R2702	R2722, R2707, R2709, R2708, R2704
DV	5	10111	R2721, R2710, R2705,R2706, R2704	R2722, R2707, R2709, R2708, R2702
PV	5	11000	R2721, R2707, R2709, R2708, R2702	R2722, R2710, R2705, R2706, R2704

TBL2702

H4GB 1866 2znm	Hynix 8Gb 1866	H9CCNNN8GTALAR-NUD
Mem	M1008409-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2711, R2712
NI	NO-STUFF	R2713, R2717, R2714, R2719, R2718
H8GB 1866 2znm	Hynix 16Gb 1866	H9CCNNNBJTALAR-NUD
Mem	M1008406-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2719, R2712
NI	NO-STUFF	R2713, R2717, R2714, R2711, R2718
S4GB 1866 D20	Samsung 8Gb 1866	K4E8E324EB-EGCF000
Mem	X946149-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2711, R2712
NI	NO-STUFF	R2713, R2716, R2714, R2719, R2718
S8GB 1866 D20	Samsung 16Gb 1866	K4E6E304EB-EGCF000
Mem	X946454-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2719, R2712
NI	NO-STUFF	R2713, R2716, R2714, R2711, R2718
S16GB 1866 D20	Samsung 32Gb 1866	K4EBE304EB-EGCF000
Mem	X930118-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2711, R2718
NI	NO-STUFF	R2713, R2716, R2714, R2719, R2712
H16GB 1866 2znm	Hynix 32Gb 1866	H9CCNNNCLGALAR-NUD
Mem	M1008421-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2711, R2718
NI	NO-STUFF	R2713, R2717, R2714, R2719, R2712



Title:	PCH(8)_HWID
Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT
Rev:	1.00
Date:	Thursday, August 03, 2017
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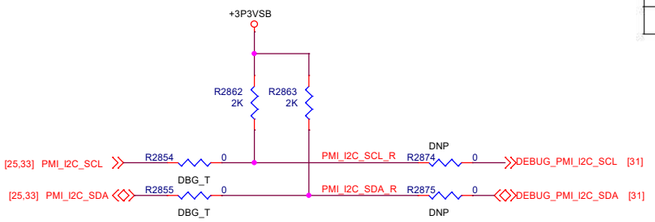
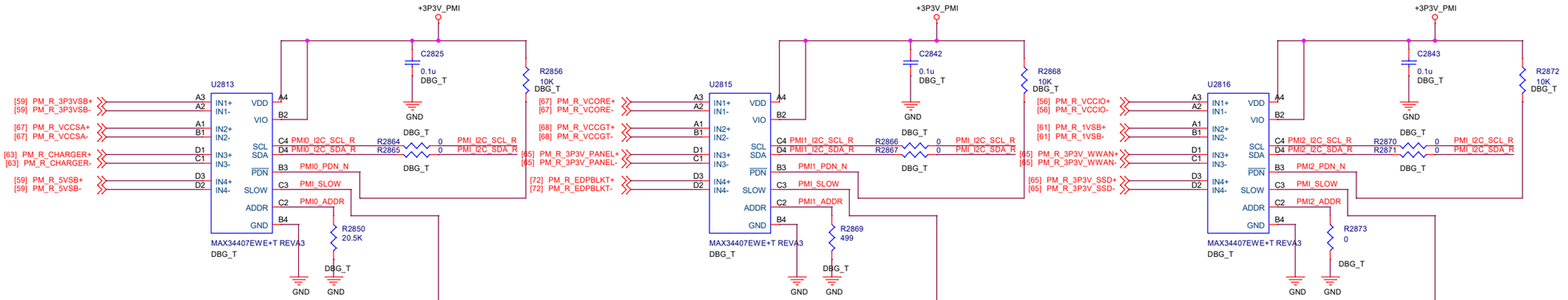
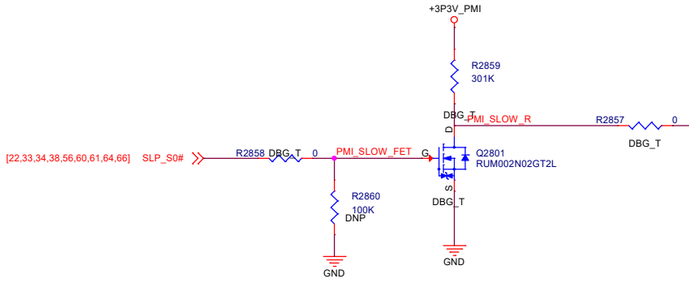
Table 5. SMBus Slave Address Select

RADDR (±1%) (kΩ)	SLAVE ADDRESS	RADDR (±1%) (Ω)	SLAVE ADDRESS
20.5	0011 110 (3Ch)	1.74k	0010 110 (2Ch)
11.0	0011 100 (38h)	931	0010 100 (28h)
5.90	0011 010 (34h)	442	0010 010 (24h)
3.16	0011 000 (30h)	Tie to GND	0010 000 (20h)



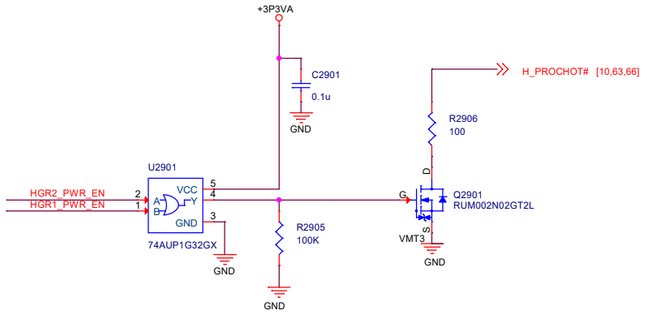


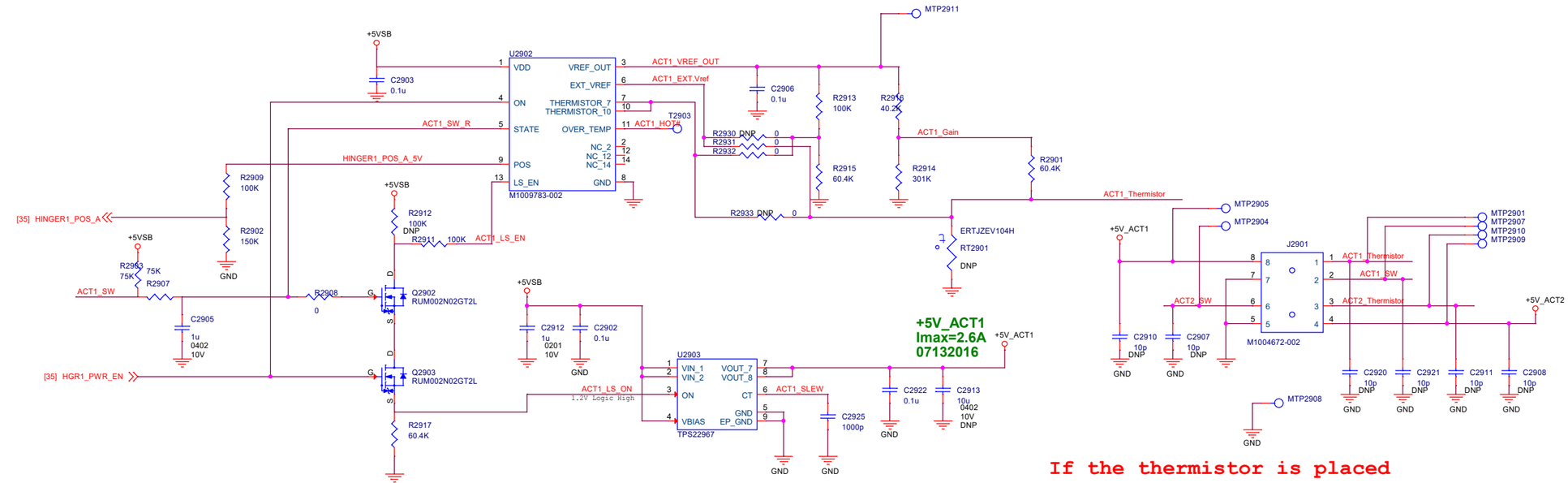


Resistor Address for MAX3440
20.5K => 2x3C/2x3D
11.0K => 2x38/2x39
5.90K => 2x34/2x35
3.16K => 2x30/2x31
1.74K => 2x2C/2x2D
931K => 2x28/2x29
499 => 2x24/2x25
GND => 2x20/2x21

Title: Power Monitor		
Engineer: <OrgAddr1>		
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 28 of 76	

ACT1 = LEFT DM
ACT2 = RIGHT DM

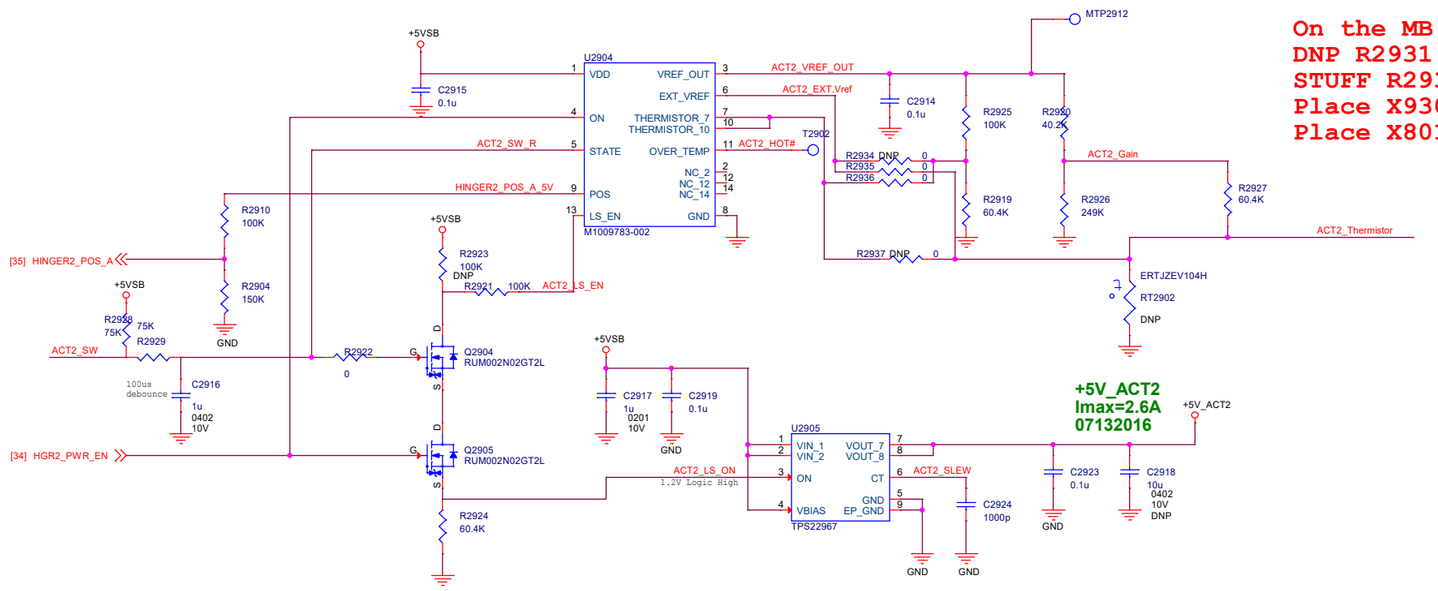




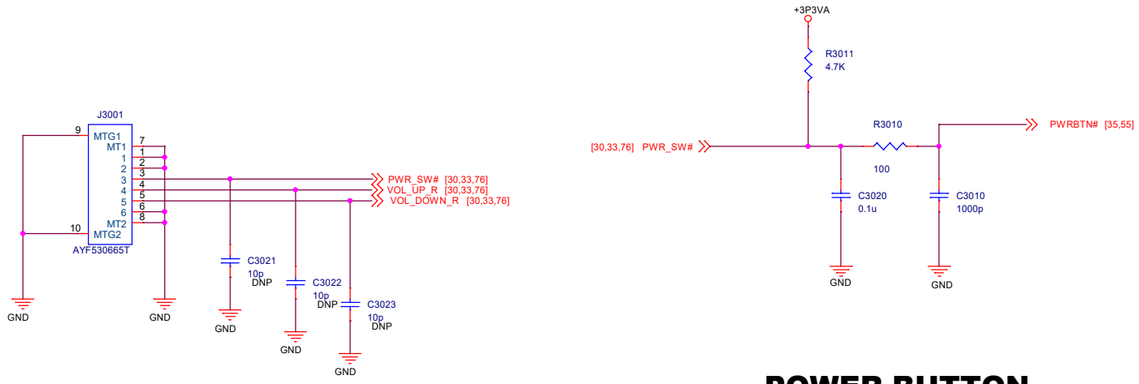
If the thermistor is placed

On the FPC: Keep everything as is

On the MB:
DNP R2931, R2932, R2935, R2936
STUFF R2930, R2933, R2934, R2937
Place X930189-001 in R2901, R2927 locations
Place X801411-001 in RT2901, RT2902 locations

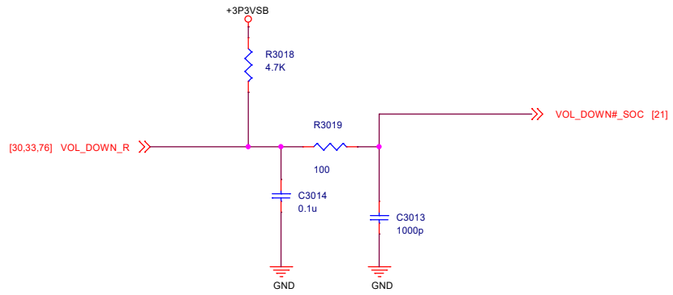


Title:	Hinger connector		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 29 of 76		

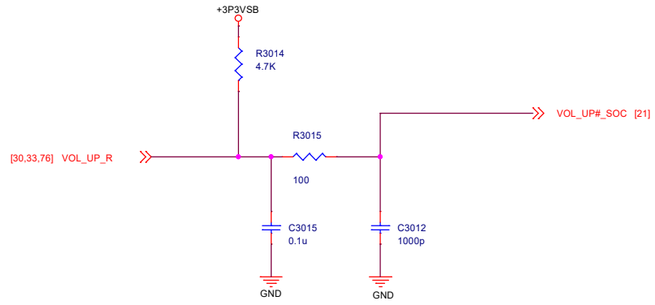


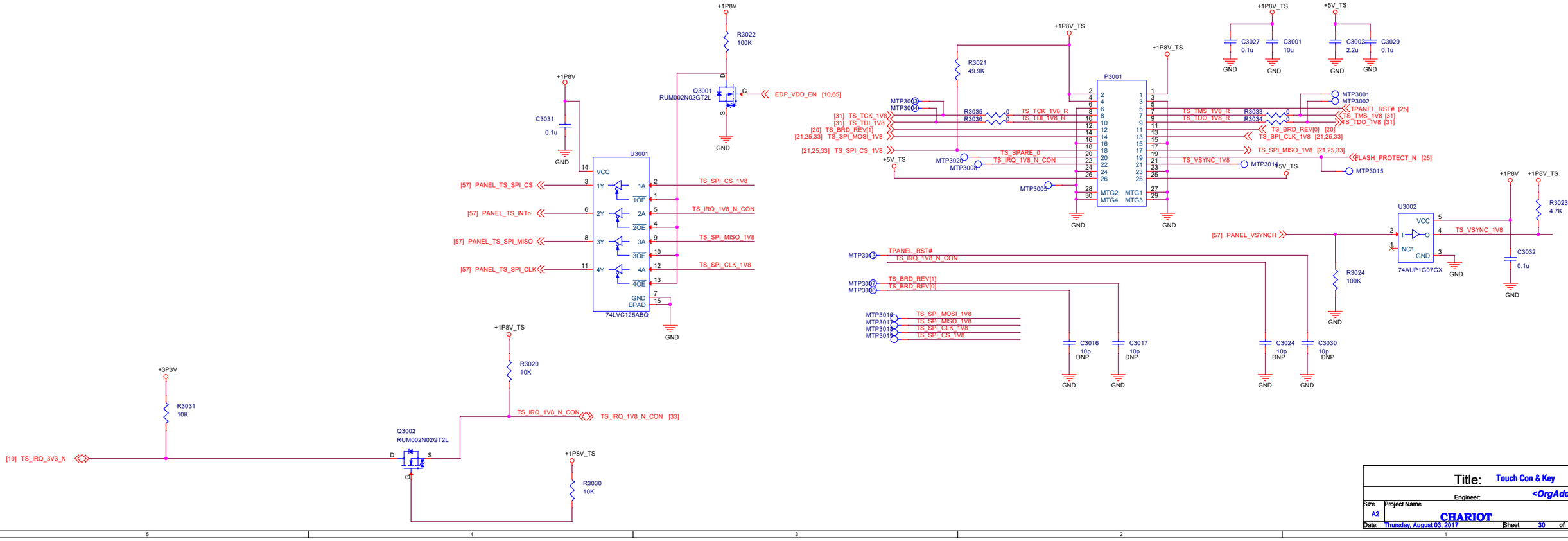
POWER BUTTON

VOL_DOWN BUTTON

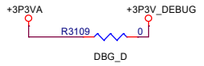


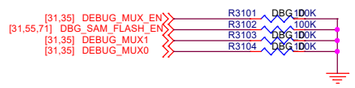
VOL_UP BUTTON

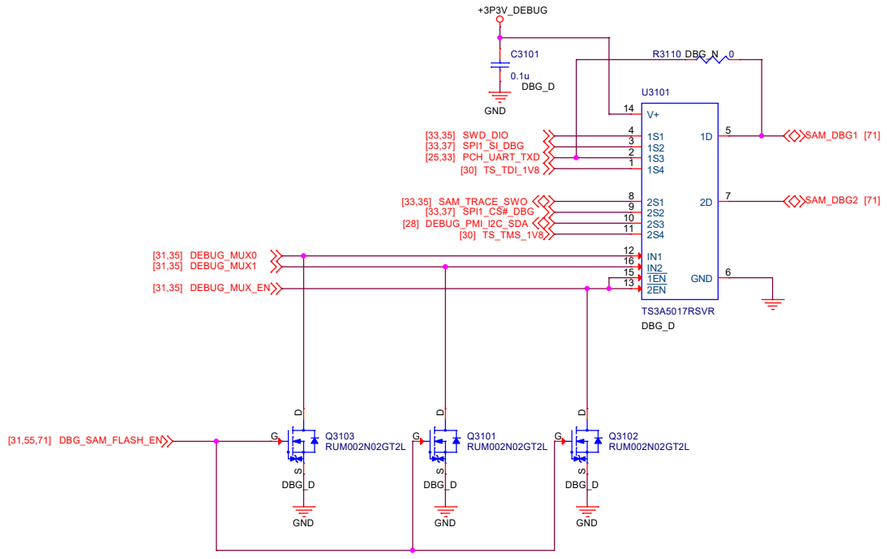


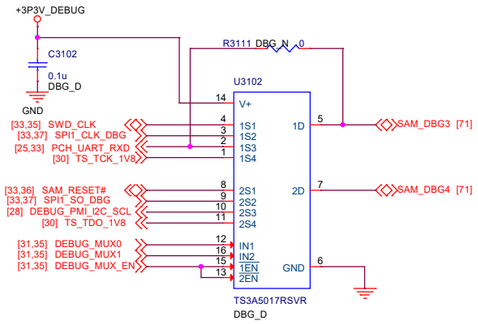


Title:	Touch Con & Key		
Engineer:	<OrgAddr1>		
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 30 of 76		









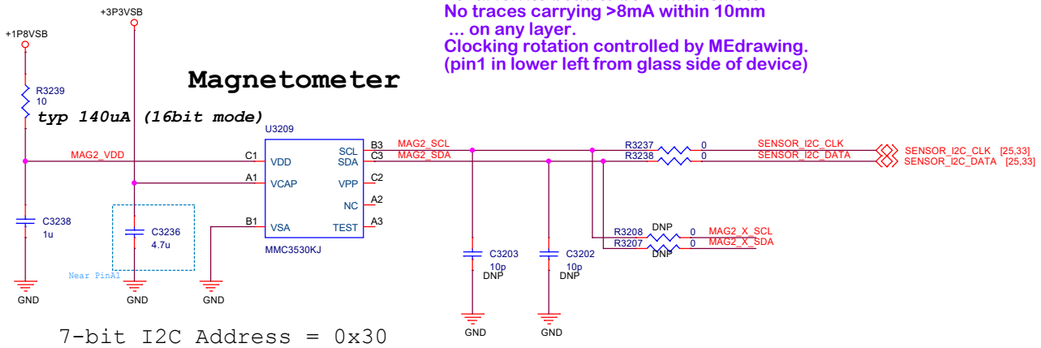
Title:	SAM Debug MUX	
Engineer:	<OrgAddr1>	
Size: A2	Project Name	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 31 of 76	

Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to to be same width,
- All traces to enter pads at zero angle.

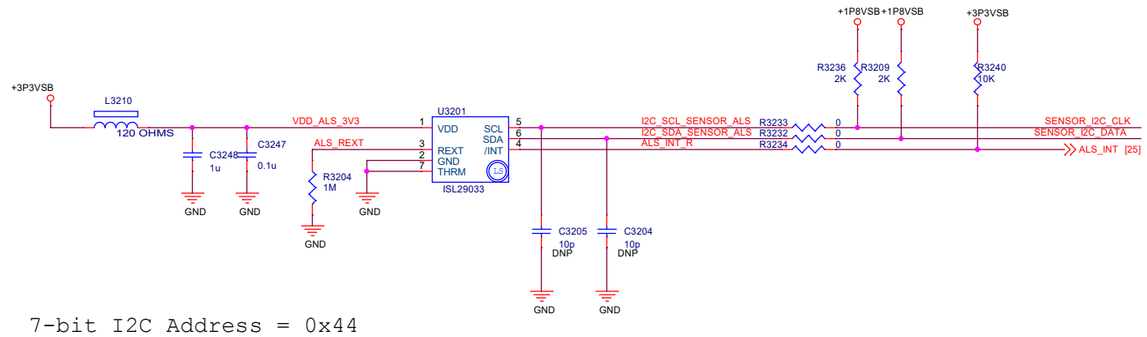
Clocking rotation controlled by MEdrawing.
(+X Device & +X Surface vectors must be parallel w/same direction
(i.e. if the part is located on the glass side of the PCB, the pin1 indicator dot should be in upper right corner)

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by MEdrawing.
(pin1 in lower left from glass side of device)

Magnetometer

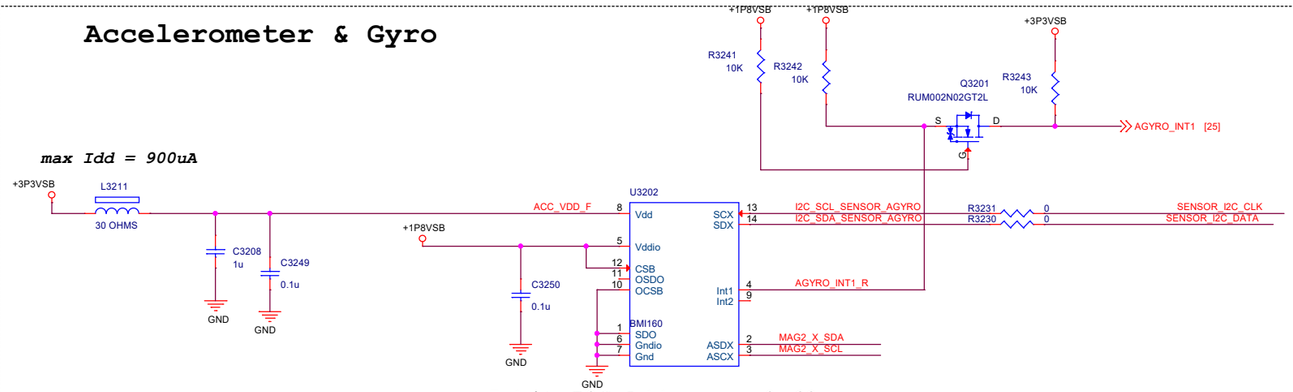


7-bit I2C Address = 0x30



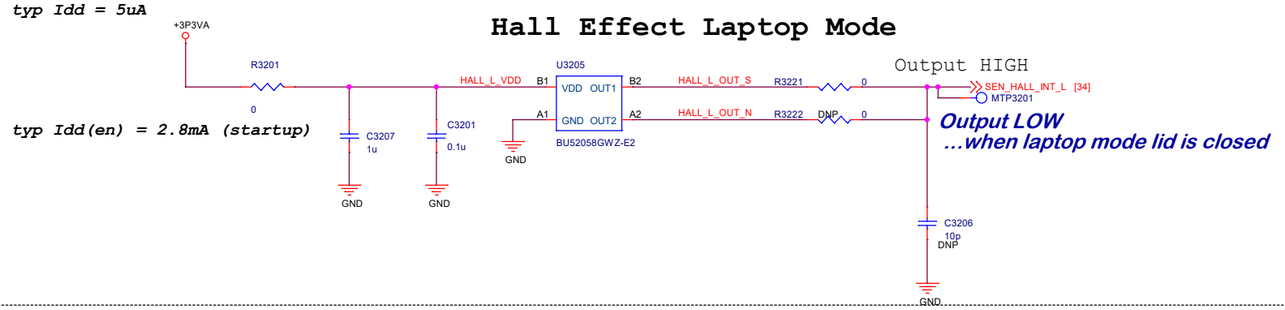
7-bit I2C Address = 0x44

Accelerometer & Gyro

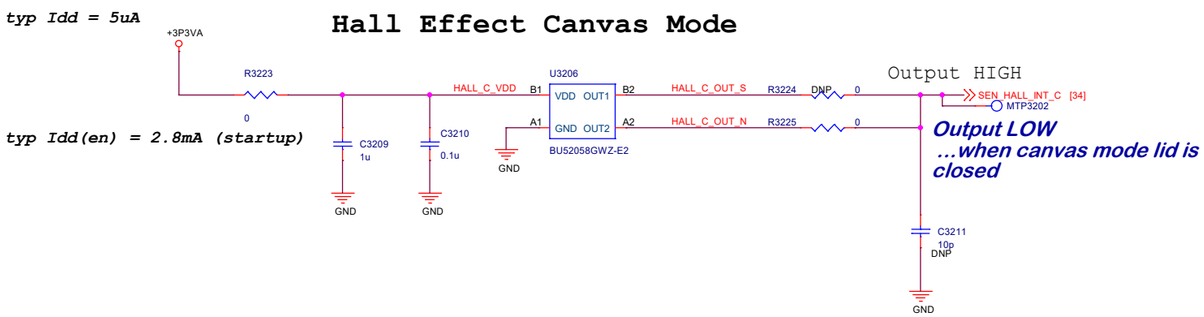


7-bit I2C Address = 0x68

Hall Effect Laptop Mode

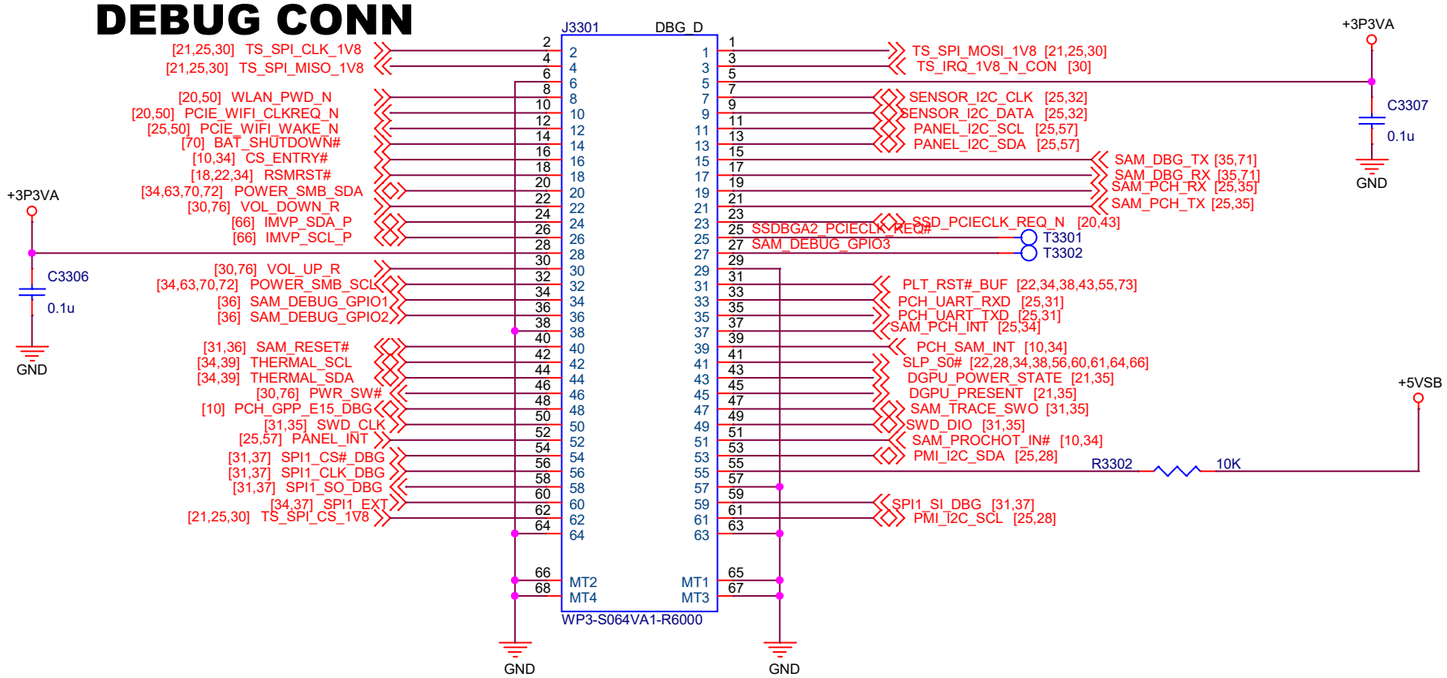


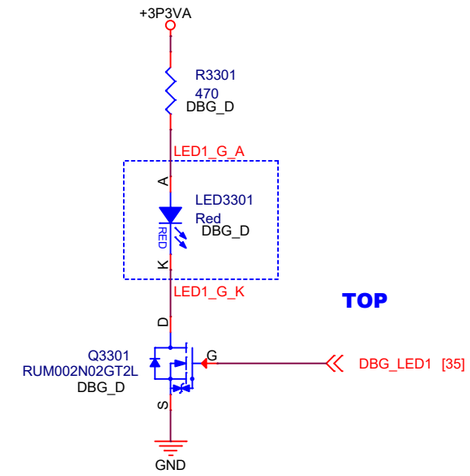
Hall Effect Canvas Mode

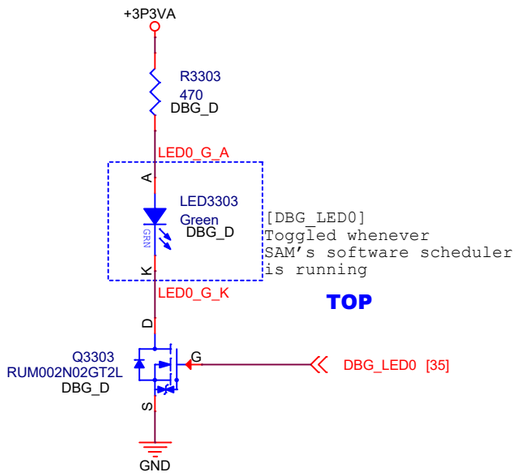


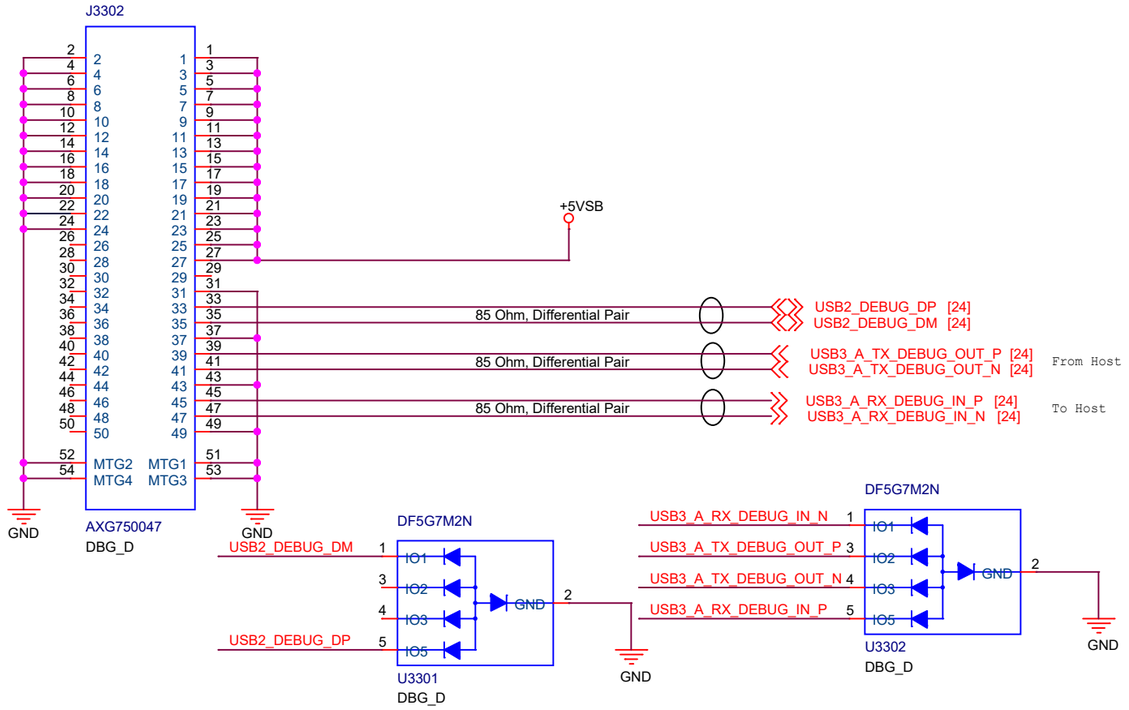
Title:	On Board-Sensors	
Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 32 of 76	

DEBUG CONN









<Core Design>

Title:	Debug Conn / LPC	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 33 of 76	

U3401A
MK22FN512VDC12

PORT A

PTA4/NMI_b/EZP_CS_b/LLWU_P3/FTM0_CH1 — J8 — TEC_BOOT_TRAP — R50150 — 100K — +3P3VA
FTM2_CH0/PTA10/FTM2_QD_PHA — J9 — SL1_HPD2_EN# [72]
PTA11/FTM2_CH1/FTM2_QD_PHB — J4 — PANEL_LOGO_PWM [72]
PTA12/FTM1_CH0/I2S0_TXD0/FTM1_QD_PHA — K8 — FAN1_PWM [39]
PTA13/LLWU_P4/FTM1_CH1/I2S0_TX_FS/FTM1_QD_PHB — L8 — SLP_S0# [22,28,33,38,56,60,61,64,66]
PTA14/SPI0_PCS0/UART0_TX/I2S0_RX_BCLK — K9 — SAM_PCH_INT [25,33]
PTA15/SPI0_SCK/UART0_RX/I2S0_RXD0 — L9 — PANEL_LOGO_BKLT_EN [72]
PTA16/SPI0_SOUT/UART0_CTS_b/I2S0_RX_FS — J10 — SL1_RX_SEL# [70]
PTA17/ADC1_SE17/SPI0_SIN/UART0_RTS_b/I2S0_MCLK — H10 — SL1_TX_SEL# [70]
PTA29/FB_A24 — H11 — ADC_RD_EN [36,70]

T3435
T3436

MK22FN512VDC12

+3P3VA
C3431 1u
C3430 0.1u
GND
GND

U3402
THERMAL_SDA — 5 SDA
THERMAL_SCL — 6 SCL
8 VCC
4 NC1
9 NC2
NC3
GND
NC7
1
2
3
7
ATECC508A-MAHUZ-T

U3401B

PORT B

PTB0/I2C0_SCL/ADC0_SE8/ADC1_SE8/LLWU_P5/FTM1_CH0/FTM1_QD_PHA — G11 — SAM_SL1_PWR_EN [63,70]
PTB1/I2C0_SDA/ADC0_SE9/ADC1_SE9/FTM1_CH1/FTM1_QD_PHB — G10 — FAN2_PWM [39]
PTB2/ADC0_SE12/I2C0_SCL/UART0_RTS_b/FTM0_FLT3 — G9 — T3417 — POWER_SMB_SCL [33,63,70,72]
PTB3/ADC0_SE13/I2C0_SDA/UART0_CTS_b/FTM0_FLT0 — G8 — T3449 — POWER_SMB_SDA [33,63,70,72]
PTB6/ADC1_SE12/FB_AD23 — F11 — SYS_PWROK [22]
PTB7/ADC1_SE13/FB_AD22 — E11 — VSUS_ON [59,61,62]
PTB8/LPUART0_RTS_b/FB_AD21 — D11 — PCH_DPWROK [22]
PTB9/SPI1_PCS1/LPUART0_CTS_b/FB_AD20 — E10 — RTCRST_CTRL [35]
PTB10/ADC1_SE14/SPI1_PCS0/LPUART0_RX/FB_AD19/FTM0_FLT1 — D10 — SAM_SPI_NPCS0 [35]
PTB11/ADC1_SE15/SPI1_SCK/LPUART0_TX/FB_AD18/FTM0_FLT2 — C10 — SAM_SPI_SPCK [35]

PTB16/SPI1_SOUT/UART0_RX/FTM_CLKIN0/FB_AD17/EWM_IN — B10 — SAM_SPI_MOSI [35]
PTB17/SPI1_SIN/UART0_TX/FTM_CLKIN1/FB_AD16/EWM_OUT_b — E9 — SAM_SPI_MISO [35]
PTB18/FTM2_CH0/I2S0_TX_BCLK/FB_AD15/FTM2_QD_PHA — D9 — ALL_SUS_PWRGD [55,61]
PTB19/FTM2_CH1/I2S0_TX_FS/FB_OE_b/FTM2_QD_PHB — C9 — SLP_SUS# [22]
PTB20/FB_AD31/CMP0_OUT — F10 — SLP_S3# [22,55]
PTB21/FB_AD30/CMP1_OUT — F9 — SLP_S4# [22,60]
PTB22/FB_AD29 — F8 — BAT_DET# [70]
PTB23/SPI0_PCS5/FB_AD28 — E8 — VRM_PWRGD [55,66]

R3439 100K
R3438 100K
GND
GND

MK22FN512VDC12

U3401C

PORT C

PTC0/ADC0_SE14/SPI0_PCS4/PDB0_EXTRG/FB_AD14/USB_SOF_OUT — B9 — T3439 — T3404 — CS_ENTRY# [10,33]
PTC1/FTM0_CH0/ADC0_SE15/LLWU_P6/SPI0_PCS3/UART1_RTS_b/FB_AD13/I2S0_TXD0/LPUART0_RTS_b — D8 — T3438 — T3403 — FAN1_TACH [39]
PTC2/ADC0_SE4b/CMP1_IN0/SPI0_PCS2/UART1_CTS_b/FTM0_CH1/FB_AD12/I2S0_TX_FS/LPUART0_CTS_b — C8 — T3402 — RSMRST# [18,22,33]
PTC3/CMP1_IN1/LLWU_P7/SPI0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/I2S0_TX_BCLK/LPUART0_RX — B8 — FAN2_TACH [39]
PTC4/LLWU_P8/SPI0_PCS0/UART1_TX/FTM0_CH3/FB_AD11/CMP1_OUT/LPUART0_TX — A8 — PCH_SAM_INT [10,33]
PTC5/LLWU_P9/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/FB_AD10/CMP0_OUT/FTM0_CH2 — D7 — SEN_HALL_INT_L [32]
PTC6/CMP0_IN0/LLWU_P10/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/FB_AD9/I2S0_MCLK — C7 — MTP3401 — SAM_PROCHOT_IN# [10,33]
PTC7/CMP0_IN1/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS/FB_AD8 — B7 — HGR2_PWR_EN_R — R3401 — 1K — T3437 — HGR2_PWR_EN [29]
PTC8/ADC1_SE4b/CMP0_IN2/FTM3_CH4/I2S0_MCLK/FB_AD7 — A7 — SLP_S3_DRV# [55,61,62,64,65]
PTC9/ADC1_SE5b/CMP0_IN3/FTM3_CH5/I2S0_RX_BCLK/FB_AD6/FTM2_FLT0 — D6 — SLP_S4_DRV# [60,61,62]
PTC10/ADC1_SE6b/I2C1_SCL/FTM3_CH6/I2S0_RX_FS/FB_AD5 — C6 — T3430 — THERMAL_SCL [33,39]
PTC11,ADC1_SE7b/LLWU_P11/I2C1_SDA/FTM3_CH7/FB_RW_b — C5 — T3431 — THERMAL_SDA [33,39]
PTC12/FB_AD27/FTM3_FLT0 — B6 — PLT_RST#_BUF [22,33,38,43,55,73]
PTC13/FB_AD26 — A6 — T3440 — R3403 — 1K — SPI1_EXT [33,37]
PTC14/FB_AD25 — A5 — VCCRTC_RST [55]
PTC15/FB_AD24 — B5 — T3442 — SB_PWRBTN# [10,22]
PTC16/LPUART0_RX/FB_CS5_b/FB_TSIZ1/FB_BE23_16_BLS15_8_b — D5 — SAM_SL1_DBG_EN [71]
PTC17/LPUART0_TX/FB_CS4_b/FB_TSIZ0/FB_BE31_24_BLS7_0_b — C4 — PANEL_LOGO_EDP_VDD_EN [65]
PTC18/LPUART0_RTS_b/FB_TBST_b/FB_CS2_b/FB_BE15_8_BLS23_16_b — B4 — SAM_PROCHOT_OUT [10]
PTC19/LPUART0_CTS_b/FB_CS3_b/FB_BE7_0_BLS31_24_b/FB_TA_b — A4 — SEN_HALL_INT_C [32]

+3P3VA
+3P3VA
R3404 2.2K
R3405 2.2K

MK22FN512VDC12

Authentication

7-bit I2C Address
= 0x60

Title:	SAM_1		
Engineer:	<OrgAddr1>		
Size: A4	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 34 of 76		

U3401D

PORT - D

PTD0/LLWU_P12/SPI0_PCS0/UART2_RTS_b/FTM3_CH0/FB_ALE/FB_CS1_b/FB_TS_b/LPUART0_RTS_b
PTD1/ADC0_SE5b/SPI0_SCK/UART2_CTS_b/FTM3_CH1/FB_CS0_b/LPUART0_CTS_b
PTD2/LLWU_P13/SPI0_SOUT/UART2_RX/FTM3_CH2/FB_AD4/I2C0_SCL/LPUART0_RX
PTD3/SPI0_SIN/UART2_TX/FTM3_CH3/FB_AD3/I2C0_SDA/LPUART0_TX
PTD4/LLWU_P14/SPI0_PCS1/UART0_RTS_b/FTM0_CH4/FB_AD2/EWM_IN/SPI1_PCS0
PTD5/ADC0_SE6b/SPI0_PCS2/UART0_CTS_b/FTM0_CH5/FB_AD1/EWM_OUT_b/SPI1_SCK
PTD6/ADC0_SE7b/LLWU_P15/SPI0_PCS3/UART0_RX/FTM0_CH6/FB_AD0/FTM0_FLT0/SPI1_SOUT
PTD7/UART0_TX/FTM0_CH7/FTM0_FLT1/SPI1_SIN
PTD8/I2C0_SCL/LPUART0_RX/FB_A16
PTD9/I2C0_SDA/LPUART0_TX/FB_A17
PTD10/LPUART0_RTS_b/FB_A18
PTD11/LPUART0_CTS_b/FB_A19
PTD12/FTM3_FLT0/FB_A20
PTD13/FB_A21
PTD14/FB_A22
PTD15/FB_A23

D4 SL1_PWR_OK [70] — T3505 — UEFI_TOP_SWAP [20]
D3
C3 SL1_UART_RX_R — R3515 100 — SAM_SL1_RX [70]
B3 SL1_UART_TX_R — R3514 100 — SAM_SL1_TX [70]
A3 BASE_PRESENT [25]
A2
B2 PANEL_LOGO [57] — SAM_PCH_RX [25,33] — R3501 100K — GND
A1 SAM_PCH_TX [25,33]
A10 R3505 1K — DEBUG_MUX_EN [31] — C3501 DNP 0.1u — GND
A9
B1 T3509 — T3507 — SL1_BUF_EN [73]
C2 BL_INST_ON — R3528 0 — BL_INST_ON_HNKSHK [10,72] — DGPU_POWER_EN [25]
C1 PCH_PWROK_SAM [55]
D2 PSU_BAT_VOL_EN [63]
D1 T3520
E1 MTP3512 — R3503 1K — DEBUG_MUX0 [31]
HINGER2_POS_A [29]

PORT - E

PTE5/SPI1_PCS2/LPUART0_RX/FTM3_CH0
PTE6/SPI1_PCS3/LPUART0_CTS_b/I2S0_MCLK/FTM3_CH1/USB_SOF_OUT
PTE24/ADC0_SE17/I2C0_SCL/EWM_OUT_b
PTE25/ADC0_SE18/I2C0_SDA/EWM_IN
PTE26/CLKOUT32K/RTC_CLKOUT/USB_CLKIN

T3501 — T3502
G4 CHRG_OK [63]
F3 LID_CLOSED [25]
H5 HGR1_PWR_EN_R — R3502 1K — MTP3503 — HGR1_PWR_EN [29]
J5 MTP3504
H6 T3508
HINGER1_POS_A [29]
R3504 1K — DEBUG_MUX1 [31]

MK22FN512VDC12

+3P3VA — T3510 — [34] SAM_SPI_NPCS

U3504

R3527 10K — 1 /CS
R3526 10K — FLASH_WP_N — 2 DO(IO1)
3 /WP
4 GND
W25X40CLUXIG

[34] SAM_SPI_MISO — T3511
GND

GND_PAD 9
VCC 8 — SAM_FLASH_VCC
/HOLD 7 — SAM_HOLD#
CLK 6 — SAM_SPI_SPCK [34]
DI(IO0) 5 — SAM_SPI_MOSI [34]

T3514
T3513
GND

+3P3VA — R3565 0 — R3525 10K
C3519 0.1u
GND

U3401F

USB0_DP F1
USB0_DM F2

ADC0_DP1 H1 — BRD_ID_BUILD [36]
ADC0_DM1 H2
ADC1_DP1/ADC0_DP2 J1 — BRD_ID_CPU [36]
ADC1_DM1/ADC0_DM2 J2
ADC0_DP0/ADC1_DP3 K1 — FTR_ID_UNITS [36]
ADC0_DM0/ADC1_DM3 K2
ADC1_DP0/ADC0_DP3 L1 — FTR_ID_TENS [36]
ADC1_DM0/ADC0_DM3 L2
ADC1_SE16/ADC0_SE22 J3
ADC0_SE16/CMP1_IN2/ADC0_SE21 H3 — SL1_ADC [70]

DAC0_OUT/CMP1_IN3/ADC0_SE23 K5 — BAT_VOL [63]
DAC1_OUT/CMP0_IN4/ADC1_SE23 K4 — PSU_VOL [63]
MTP_BF3532
GND — MTP_BF3531
MTP_BF3530

JTAG_TCLK/PTA0/SWD_CLK/EZP_CLK/UART0_CTS_b/FTM0_CH5 J6 — SWD_CLK [31,33]
JTAG_TDI/PTA1/EZP_DI/UART0_RX/FTM0_CH6 H8 — DGPU_PRESENT [21,33]
JTAG_TDO/PTA2/TRACE_SWO/EZP_DO/UART0_TX/FTM0_CH7 J7 — SAM_TRACE_SWO [31,33]
JTAG_TMS/PTA3/SWD_DIO/UART0_RTS_b/FTM0_CH0 H9 — SWD_DIO [31,33]
JTAG_TRST_b/PTA5/USB_CLKIN/FTM0_CH2/I2S0_TX_BCLK K7 — DGPU_POWER_STATE [21,33]

PTE0/CLKOUT32K/I2C1_SDA/ADC1_SE4a/SPI1_PCS1/UART1_TX/RTC_CLKOUT E4 — SAM_DEBUG_UART_TX_R — 33 R3543 — MTP3528 — SAM_DBG_TX [33,71]
PTE1/I2C1_SCL/ADC1_SE5a/LLWU_P0/SPI1_SOUT/UART1_RX/SPI1_SIN E3 — SAM_DEBUG_UART_RX_R — 33 R3544 — SAM_DBG_RX [33,71]
PTE2/ADC1_SE6a/LLWU_P1/SPI1_SCK/UART1_CTS_b E2 — DBG_LED1 [33] — MTP3529
PTE3/ADC1_SE7a/SPI1_SIN/UART1_RTS_b/SPI1_SOUT F4 — DBG_LED0 [33]
PTE4/LLWU_P2/SPI1_PCS0/LPUART0_TX H7 — PWRBTN# [30,55]

Debug UART to SL1

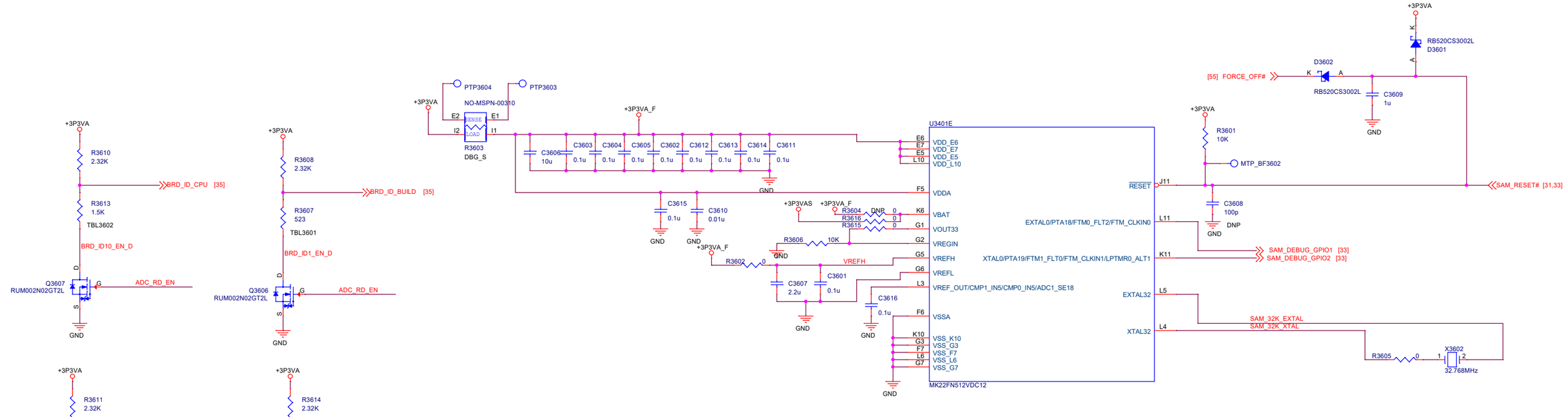
RTC_WAKEUP L7
NC_B11 B11
NC_C11 C11
NC_A11 A11
NC_K3 K3
NC_H4 H4

MK22FN512VDC12

T3521 — R3569 0 — [34] RTCRST_CTRL — RTCRST_CTRL_FET
Q3501 RUM002N02GT2L (D, G, S) — RTC_RST# [20]
R3567 100K
GND — GND

	HINGER1_POS_A_R	HINGER1_POS_B_R
Closed	High	Low
Transition	High	High
Open	Low	High
fault	Low	Low

Title:	SAM_2		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 35 of 76		



TBL3601

Build	R3607	MSPN
	80.6	X860461-001
EV3A	169	X909593-001
EV3B	267	X806948-001
DV	383	X807226-001
PV	523	X800457-001

TBL3602

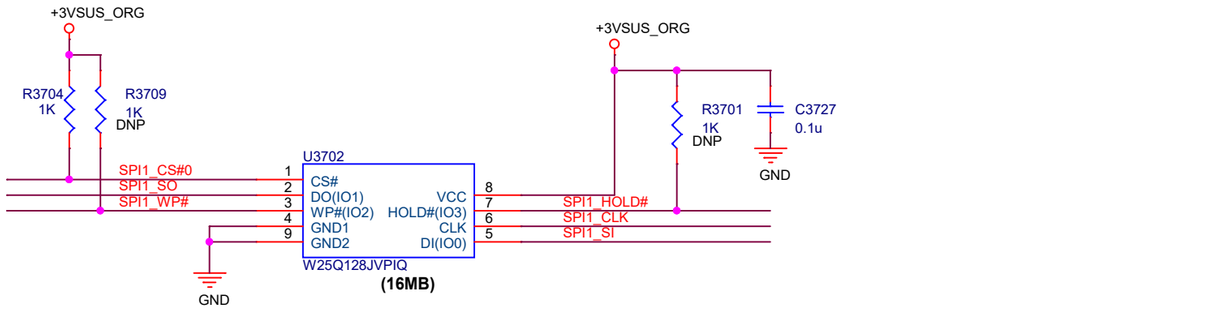
Proc Type	R3613	MSPN
Y	80.6	X860461-001
U22 i5	169	X909593-001
U22 i7	267	X806948-001
U23e	383	X807226-001
H42 i5	523	X800457-001
H42 i7	698	X853019-001
H44e	909	X807179-001
U42 i5	1180	X804207-001
U42 i7	1500	X806696-001

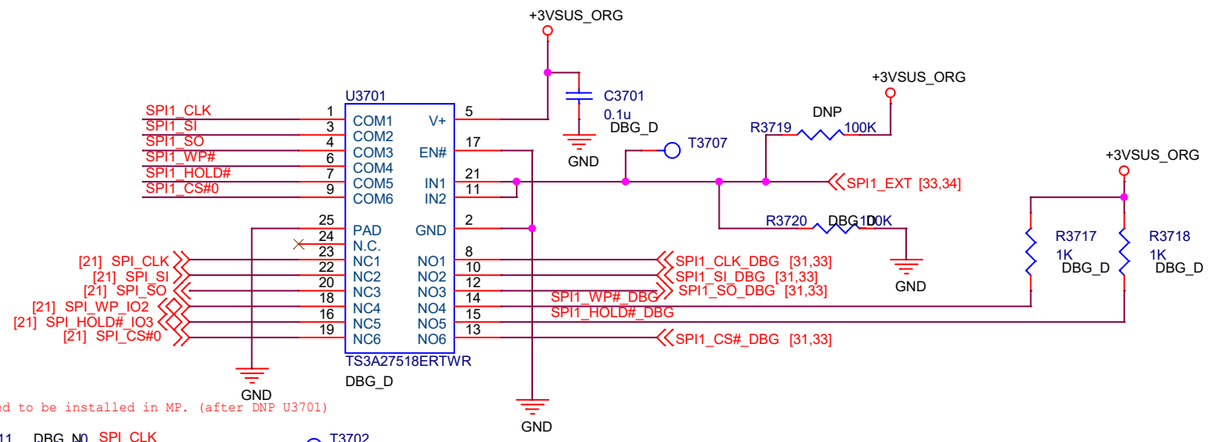
TBL3603

Build	R3609	MSPN
Gauntlet	1500	X806696-001
Shield	2000	X800427-001

DGPU_PRESENT. Driven by SAM. This will indicate the presence of dGPU (1) or not (0).
DGPU_POWER_STATE. Driven by SAM. This will indicate that the dGPU is powered up (1) or not (0). DGPU_POWER_STATE is always 0 when DGPU_PRESENT is 0.
DGPU_POWER_EN. Driven by PCH. This will request dGPU power to be turned on (1) or off (0). DGPU_POWER_EN is always 0 when DGPU_PRESENT is 0

Title:	SAM_3_PWR_IO_ID		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 36 of 76		



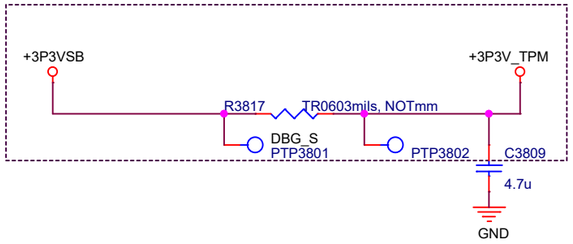


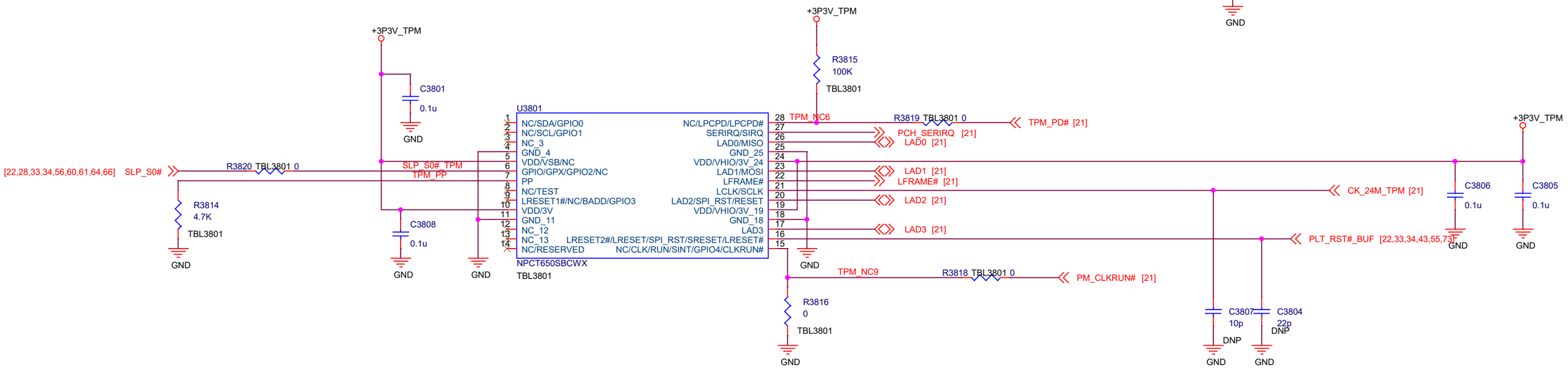
BW=200MHz

EN#	IN1/IN2	FUNCTION
L	L	COM to NC
L	H	COM to NO
H	X	Disconnect

Title: UEFI SPI ROM			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 37 of 76		

Trusted Platform Module





NationZ Z32H320TC do not support CLKRUN# and LPCPD# function
IFX don't have PP funcation in TPM2.0

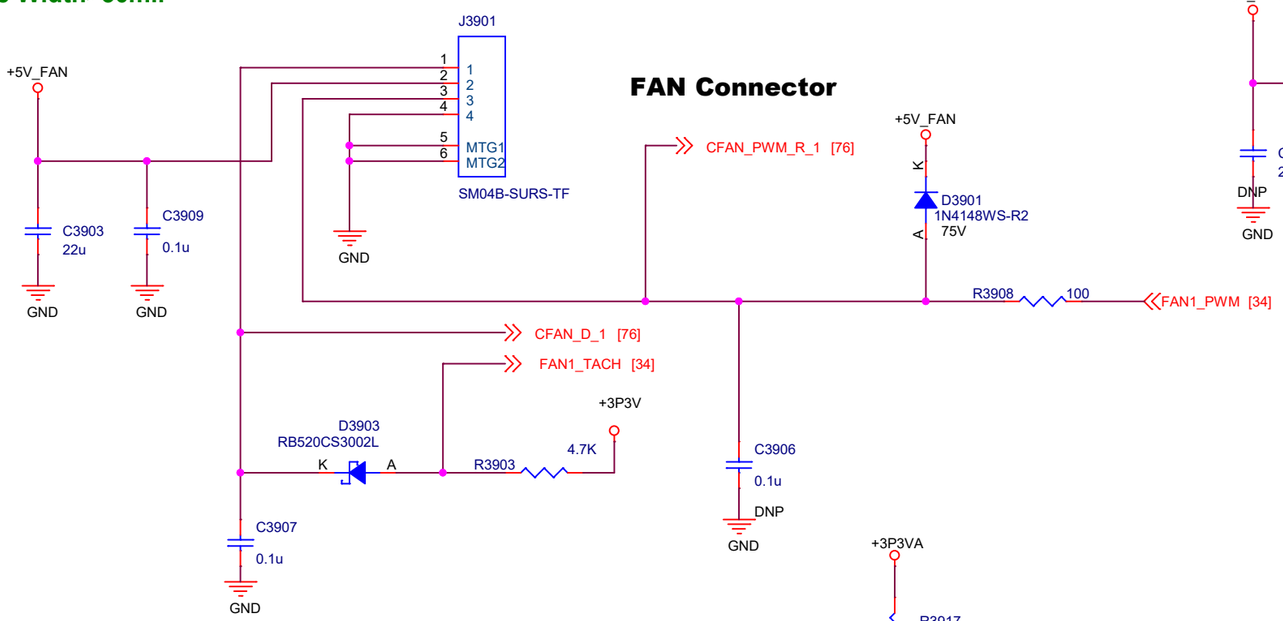
TBL3801

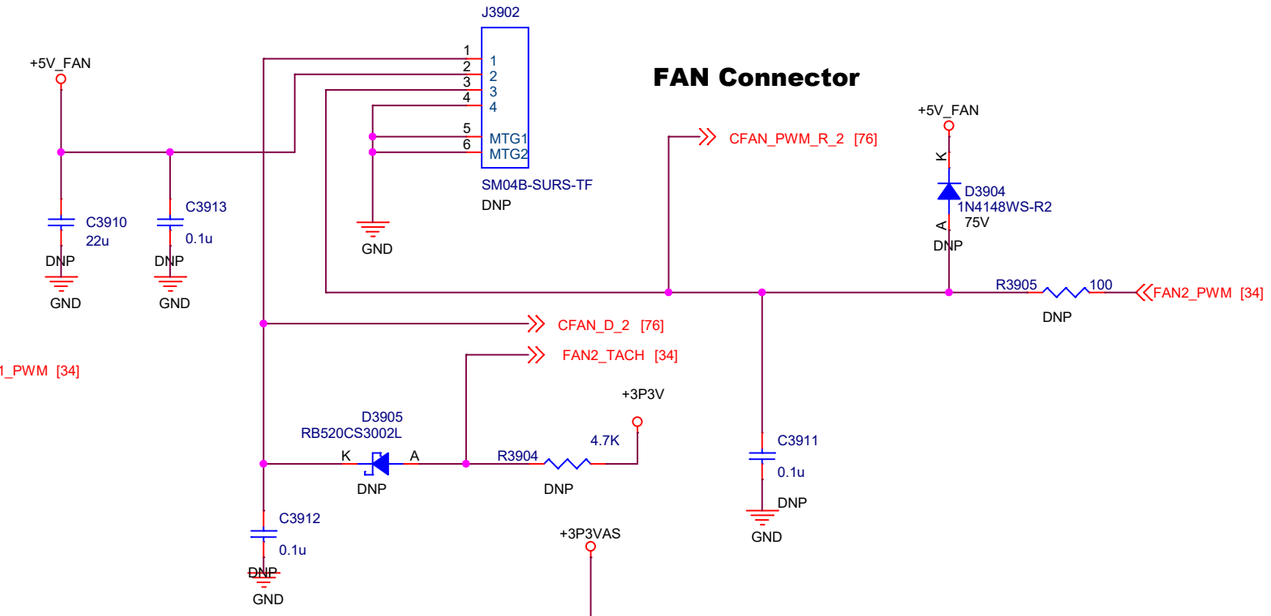
Ref	Infineon	NationZ	Nuvoton
R2701	X811791-001	NO-STUFF	X811791-001
R2703	NO-STUFF	X811791-001	NO-STUFF
R3814	X852314-001	NO-STUFF	X852314-001
R3815	NO-STUFF	X813010-001	NO-STUFF
R3816	NO-STUFF	X811786-001	NO-STUFF
R3818	NO-STUFF	NO-STUFF	X811786-001
R3819	NO-STUFF	NO-STUFF	X811786-001
R3820	NO-STUFF	NO-STUFF	X811786-001
U3801	X912460-002	X930840-002	M1006791-003

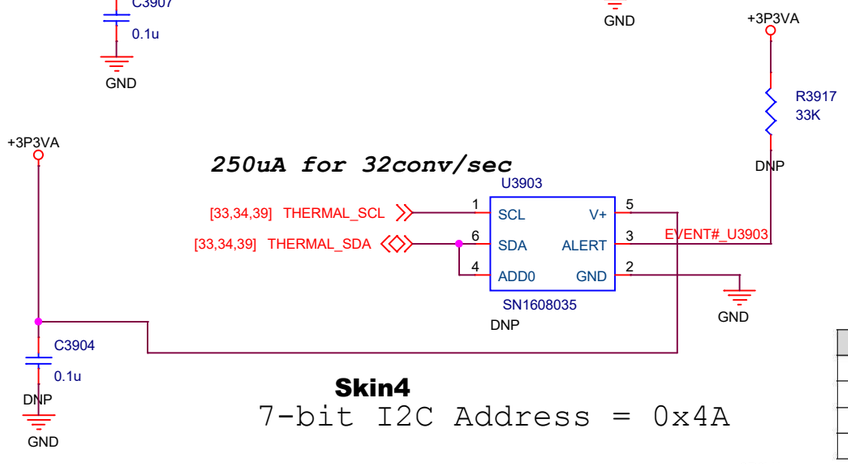
Title:	TPM	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 38 of 76	

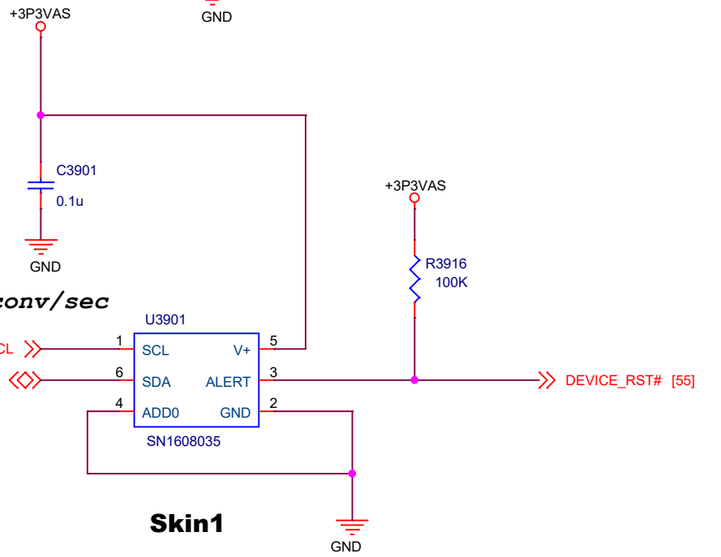
+5V_FAN
Imax=0.7A
Trace Width>30mil

FAN Connector

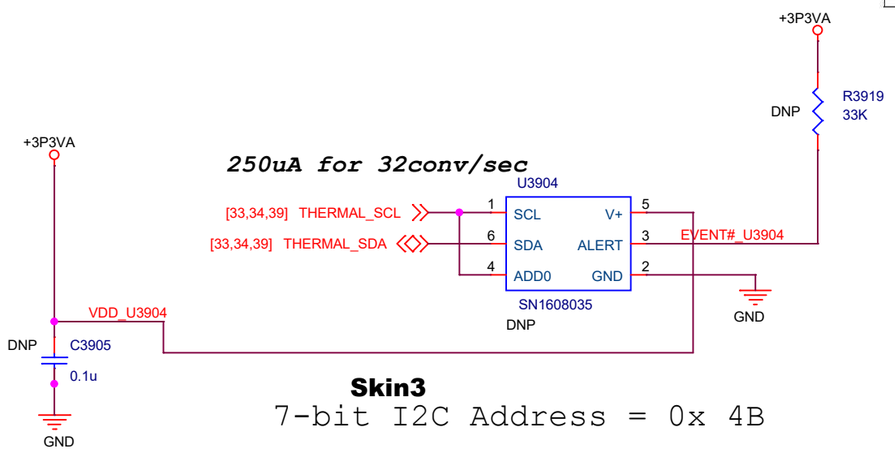


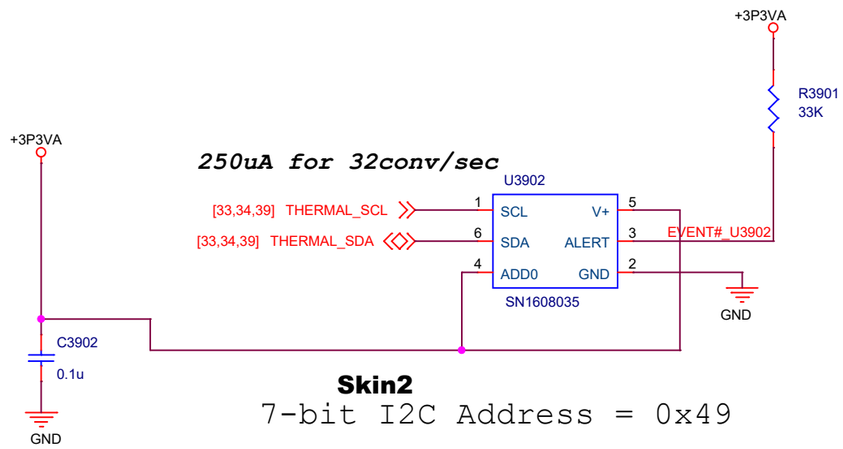






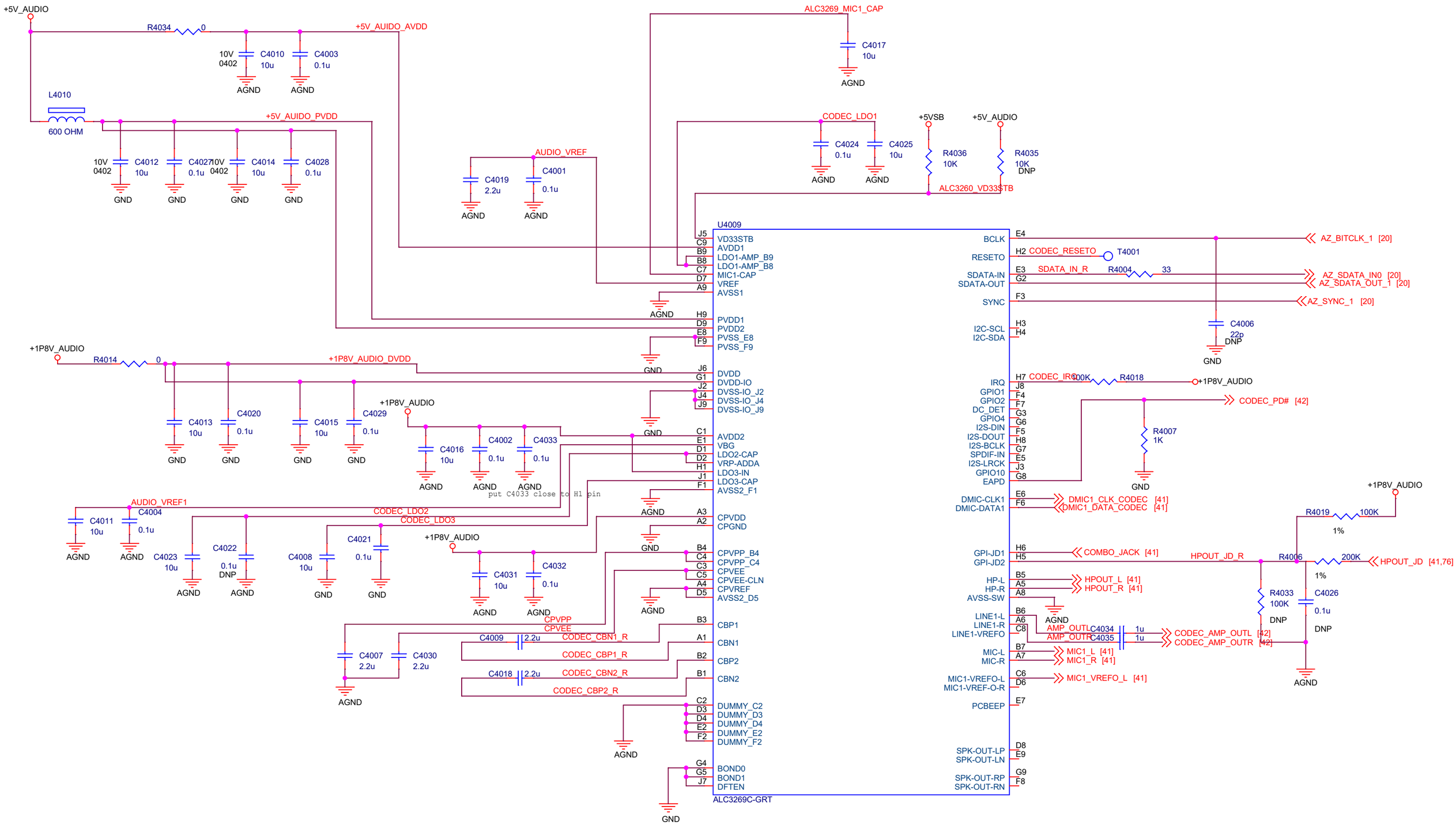
DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL





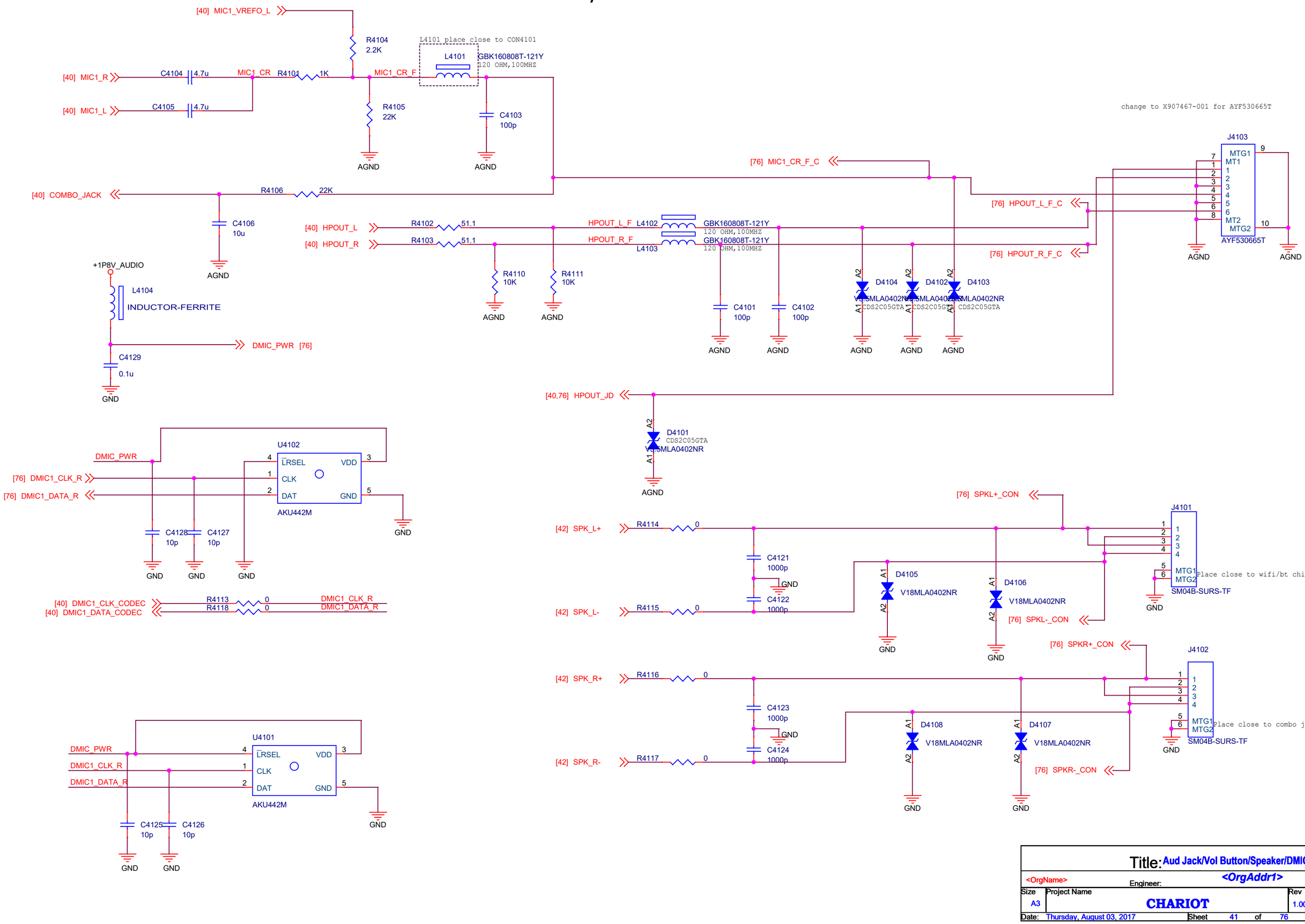
temp sensor for the right location testing

Title:	Temp Sensor/System Fan	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 39 of 76	



Title:	Realtek ALC3269 CODEC	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 40 of 76	

HP/MIC1 Combo Jack

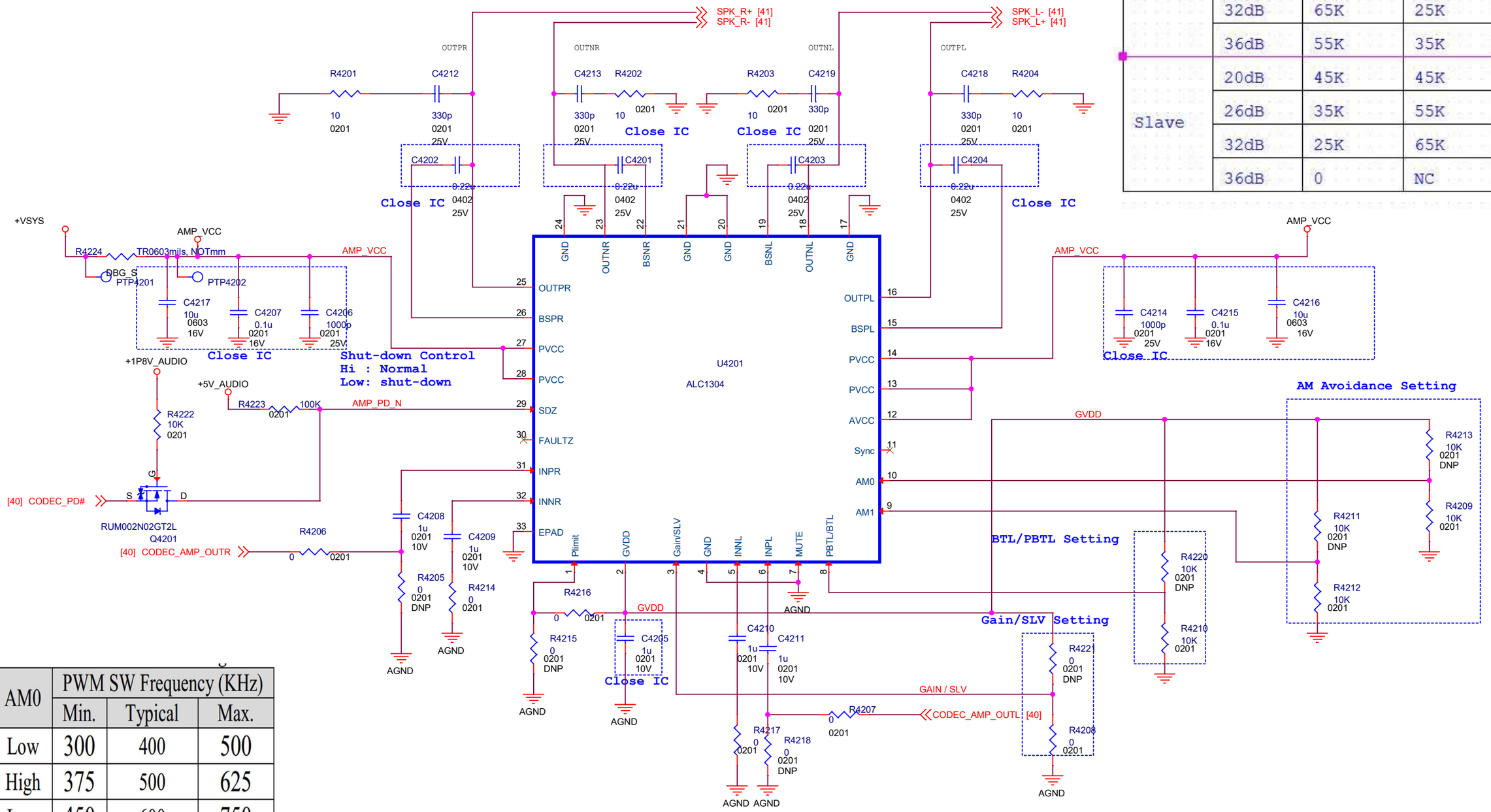


Title: Aud Jack/Vol Button/Speaker/DMIC			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 41 of 76		

Stereo Input(S.E.)
Stereo Output-BTL

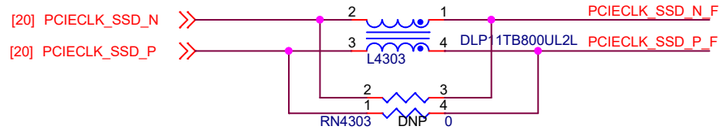
SPKR Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

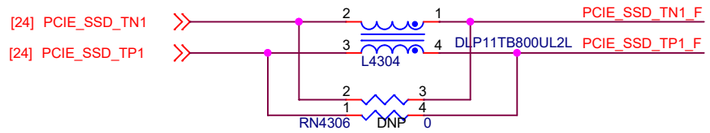
Mode	Gain	R4221 RX(ohm)	R4208 RY(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC

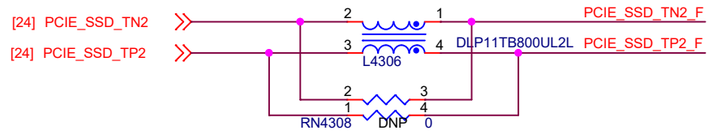


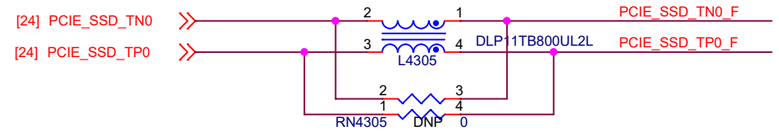
AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

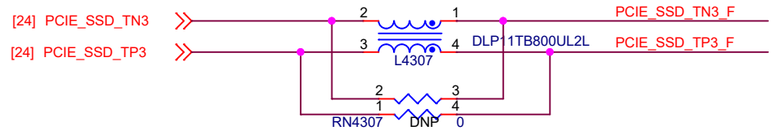
Title:	Speaker AMP		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 42 of 76		

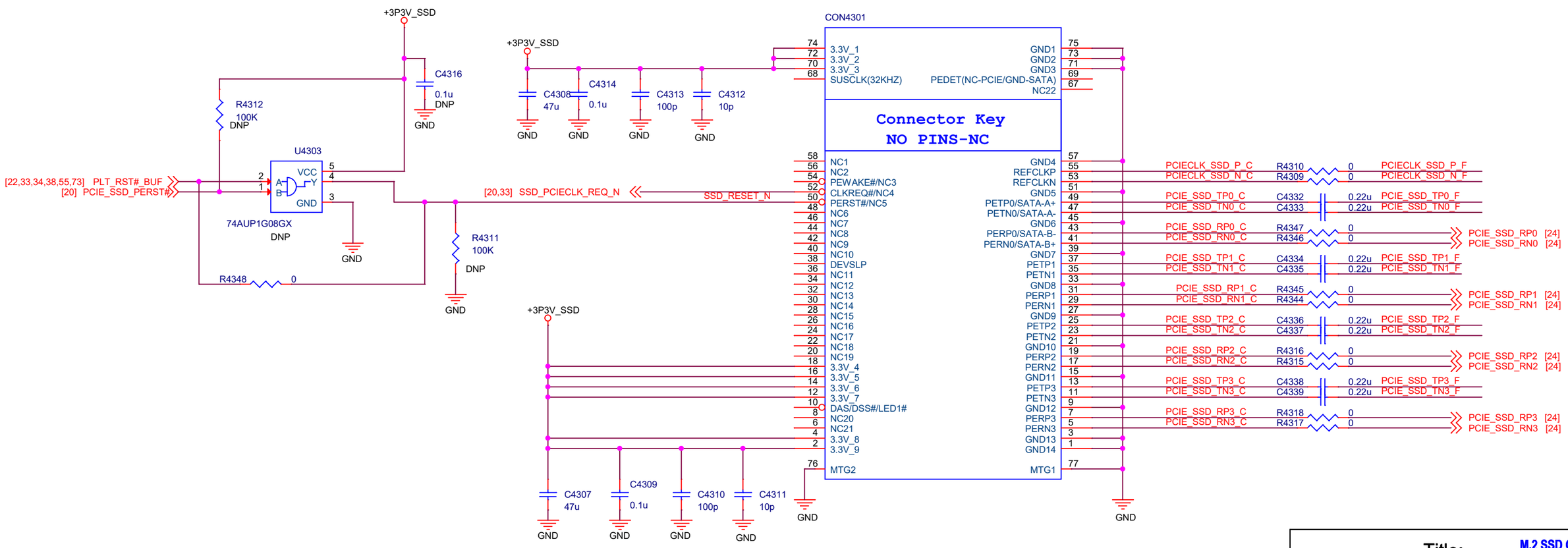






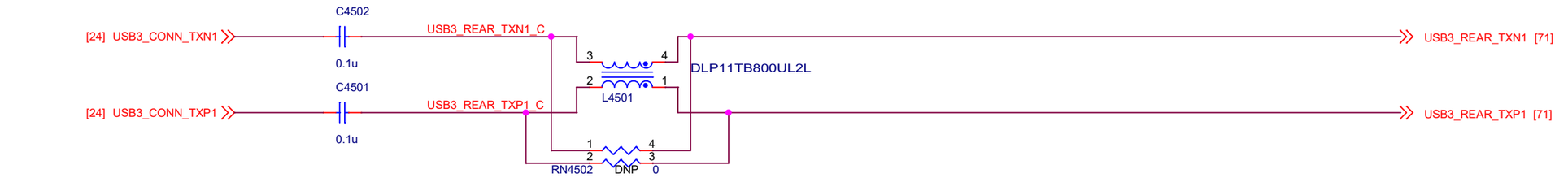


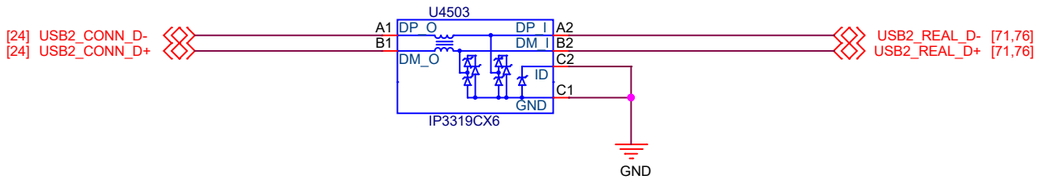




Title:	M.2 SSD CONNECTOR		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 43 of 76		

Title:				X
<OrgName>	Engineer:			<OrgAddr1>
Size: A3	Project Name: CHARIOT			Rev: 1.00
Date: Thursday, August 03, 2017		Sheet 44 of 76		



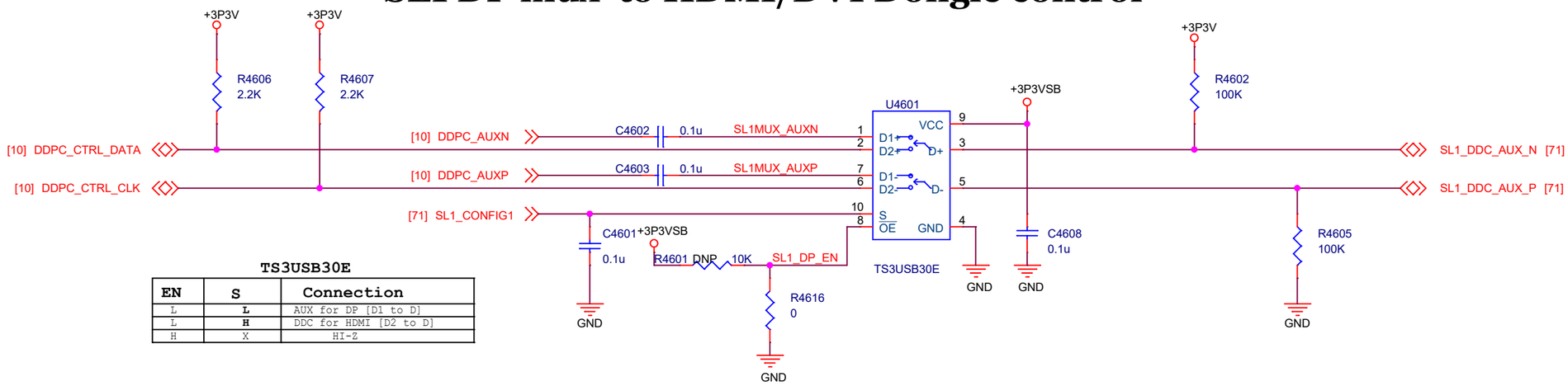


Note: IP3319CX6 D+ and D- is interchageable as seen in data sheet. Flipped for layout convenience.

Title:	USB3.0	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 45 of 76	

when you TI ts3usb30e (X870617-001), NIR4613 and R4601 and install R4615 and R4616

SL1 DP mux to HDMI/DVI Dongle control



TS3USB30E

EN	S	Connection
L	**L**	AUX for DP [D1 to D]
L	**H**	DDC for HDMI [D2 to D]
H	X	HI-Z

Title:	DP Dongle Control	
<OrgName>	Engineer:	*<OrgAddr1>*
Size: A3	Project Name: **CHARIOT**	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 46 of 76	

MP4701 MP4702 MP4703 MP4704 MP4705
FSNR_KNURL FSNR_KNURL FSNR_KNURL FSNR_KNURL FSNR_KNURL
GND GND GND GND GND

MP4706 MP4707 MP4708 MP4709 MP4710
FSNR_KNURL FSNR_KNURL FSNR_KNURL FSNR_KNURL FSNR_KNURL
GND GND GND GND GND

MP4711 MP4712 MP4713
FSNR_KNURL FSNR_KNURL FSNR_KNURL
GND GND GND

MP4714 MP4715 MP4716 MP4717 MP4718
M1005078-001 M1005078-001 M1005078-001 M1005078-001 M1005078-001
GND GND GND GND GND

J4701 J4702 J4703 J4704 J4705 J4706 J4707
M1007925-001 M1007925-001 M1007925-001 M1007925-001 M1007925-001 M1007925-001 M1007925-001
GND GND GND GND GND GND GND

PEMNUTfor XDP
MP4719
INSERT
GND

X4709
SHIELD
M1008861-001
ZID = 00
ZOD = 00
GND FRM,SHIELD H,AL

X4706
SHIELD
M1008858-002
ZID = 00
ZOD = 00
GND FRM,SHIELD G,AL

X4707
SHIELD
M1008856-002
ZID = 000
ZOD = 000
GND FRM,SHIELD F,AL

J4708
M1008639-002
GND

J4709
M1008640-002
GND

J4710
M1008641-002
GND

X4711
SHIELD
M1008863-002
ZID = 00
ZOD = 00
GND FRM,SHIELD I,AL

X4708
SHIELD
M1008850-001
ZID = 00
ZOD = 00
GND FRM,SHIELD C,AL

X4710
SHIELD
M1008864-001
ZID = 000
ZOD = 000
GND SHLD,RAM SHIELD FRAME,AL

X4705
SHIELD
M1008852-001
DNP
ZID = 00
ZOD = 00
GND FRM,SHIELD D1,AL

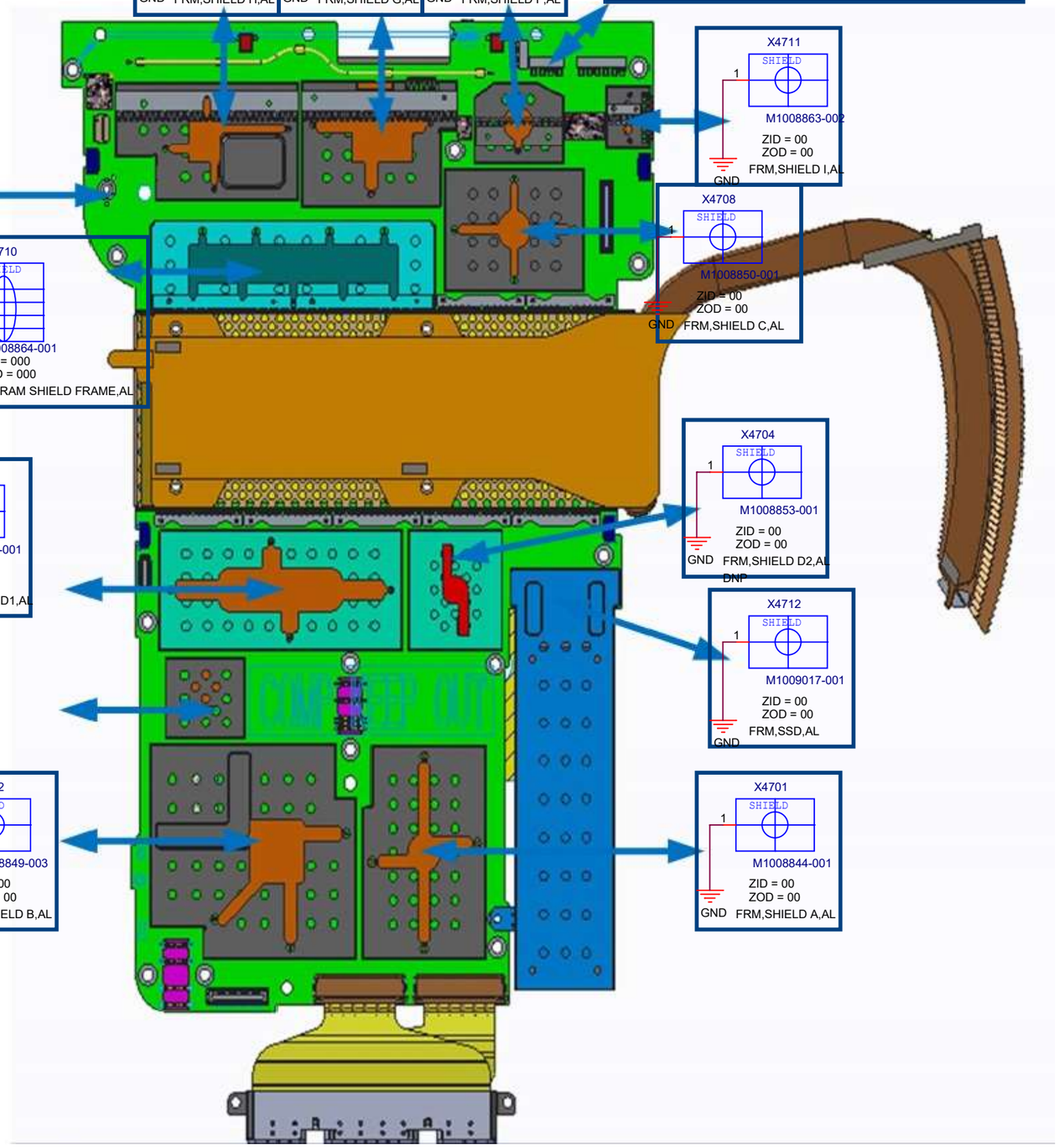
X4703
SHIELD
M1008850-001
ZID = 00
ZOD = 00
GND FRM,SHIELD C,AL

X4702
SHIELD
M1008849-003
ZID = 00
ZOD = 00
GND FRM,SHIELD B,AL

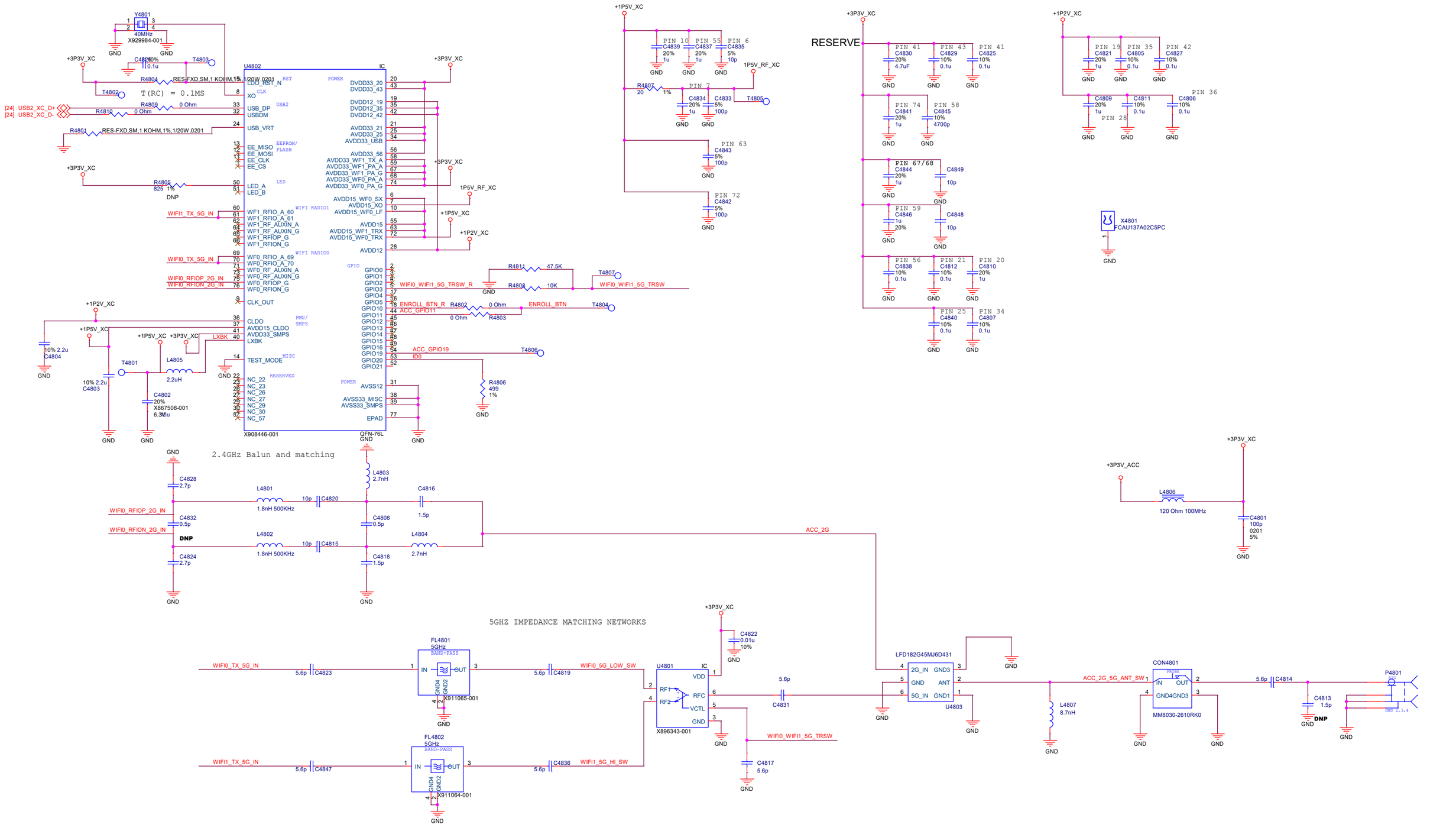
X4704
SHIELD
M1008853-001
ZID = 00
ZOD = 00
GND FRM,SHIELD D2,AL
DNP

X4712
SHIELD
M1009017-001
ZID = 00
ZOD = 00
GND FRM,SSD,AL

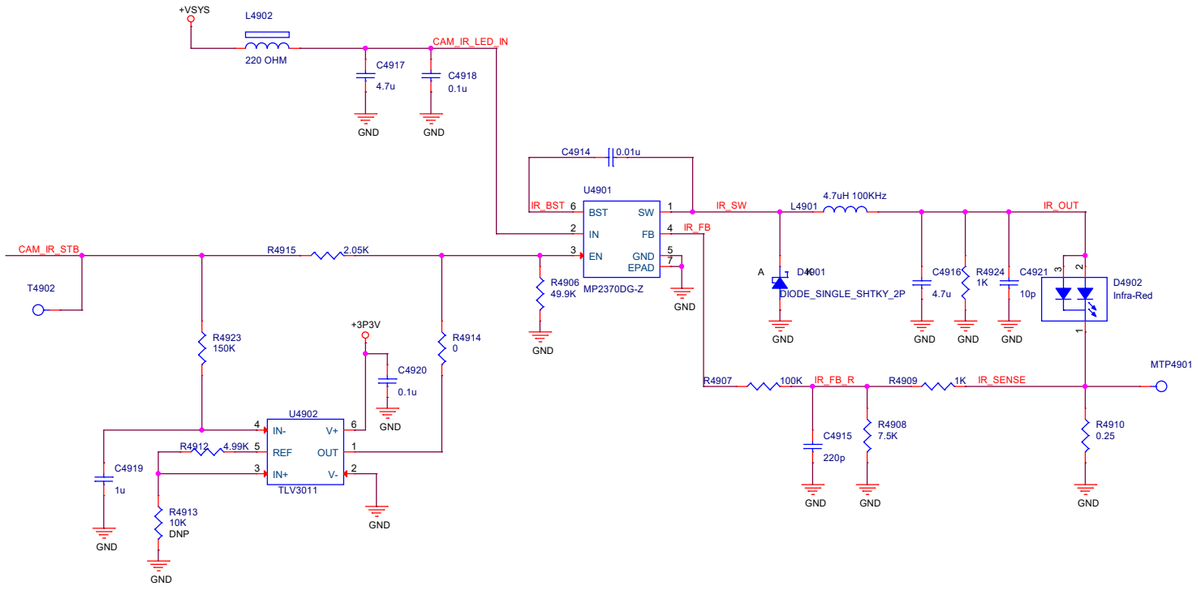
X4701
SHIELD
M1008844-001
ZID = 00
ZOD = 00
GND FRM,SHIELD A,AL

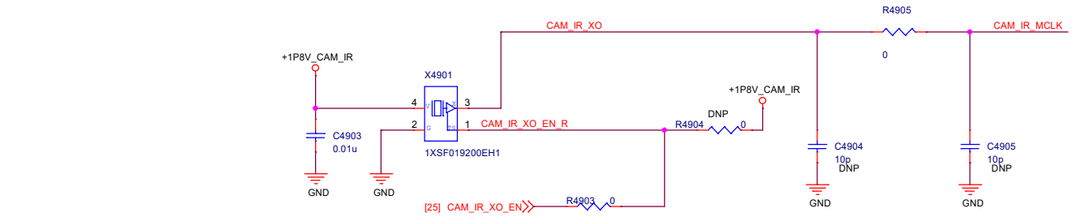


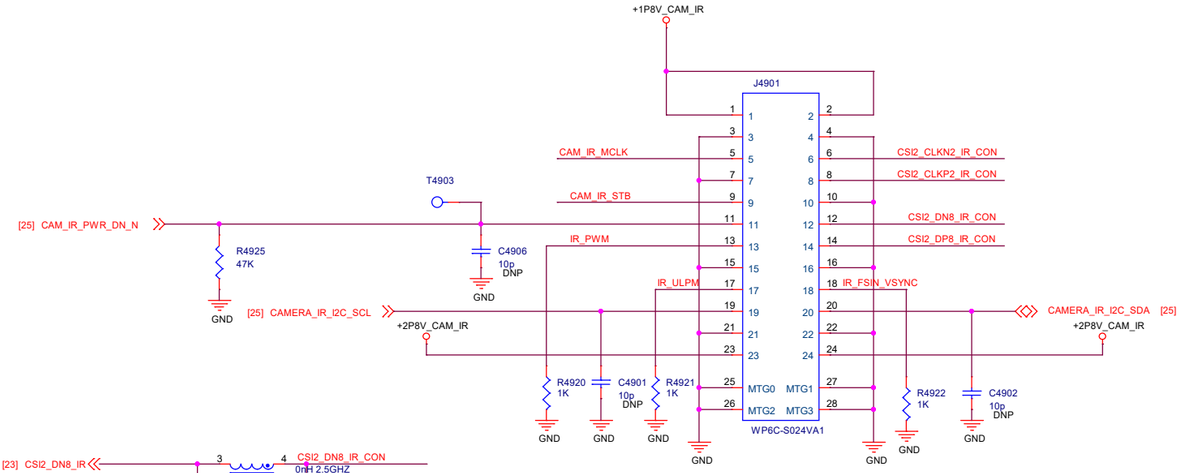
Title:	ME Parts		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 47 of 76		

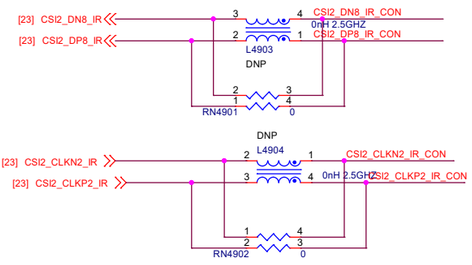


Title:	ACC Radio		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 48 of 76		

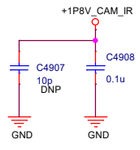


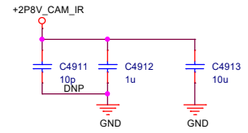




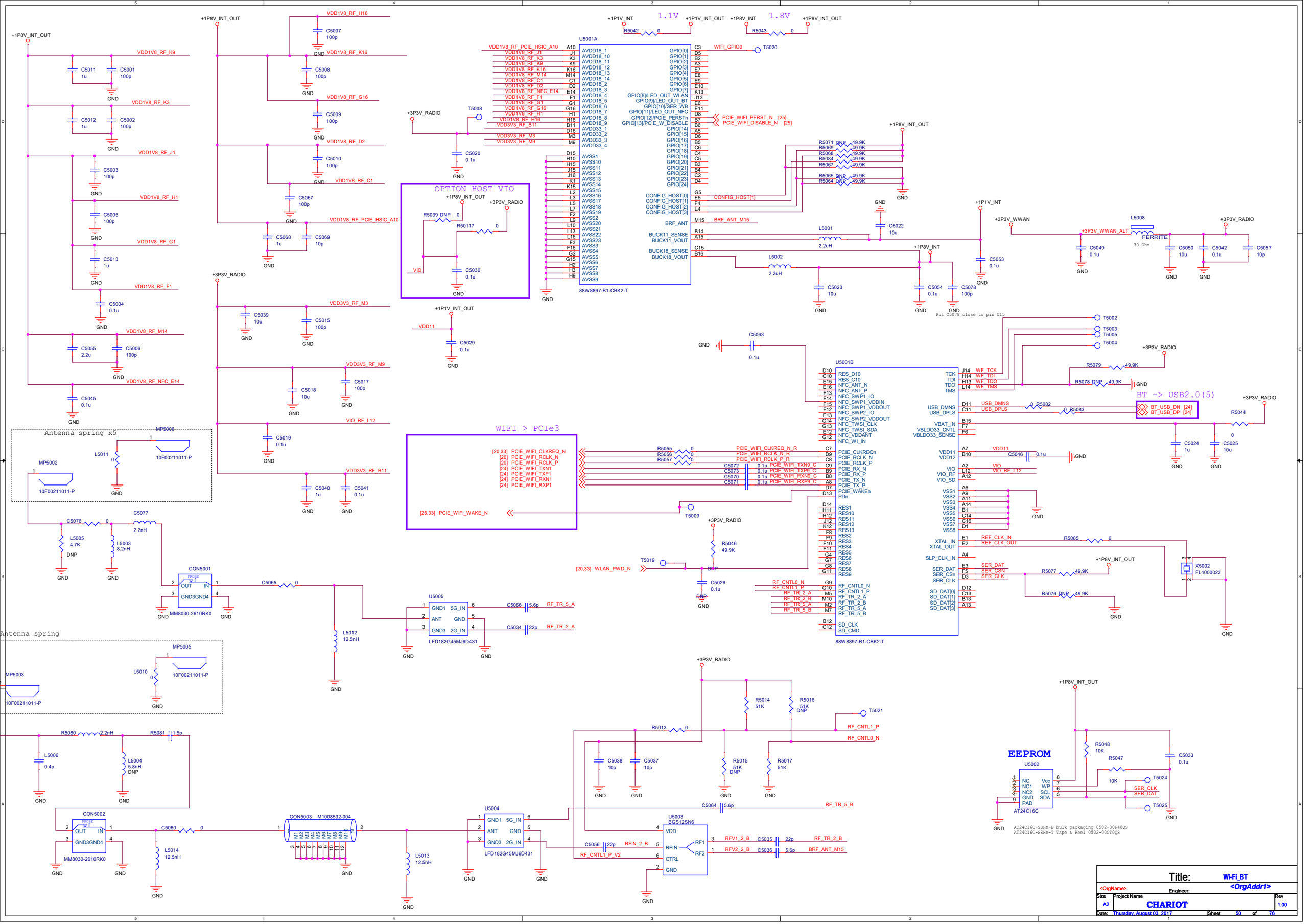


7-bit I2C Address = 0X60





Title:	IR Cam		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 49 of 76		


+1P8V_INT_OUT
VDD1V8_RF_K9
C5011 1u
C5001 100p
GND
VDD1V8_RF_K3
C5012 1u
C5002 100p
VDD1V8_RF_J1
C5003 100p
VDD1V8_RF_H1
C5005 100p
VDD1V8_RF_G1
C5013 1u
VDD1V8_RF_F1
C5004 0.1u
VDD1V8_RF_M14
C5055 2.2u
C5006 100p
VDD1V8_RF_NFC_E14
C5045 0.1u
Antenna spring x5
MP5006
L5011 0
10F00211011-P
MP5002
C5077
C5076 0
2.2nH
L5005 4.7K DNP
L5003 8.2nH
CON5001
MM8030-2610RK0
C5065 0
L5012 12.5nH
Antenna spring
MP5005
L5010 0
MP5003
R5080 2.2nH
R5081 1.5p
L5006 0.4p
L5004 5.8nH DNP
CON5002
C5060 0
L5014 12.5nH
CON5003 M1008532-004
L5013 12.5nH
+1P8V_INT_OUT
VDD1V8_RF_H16
C5007 100p
VDD1V8_RF_K16
C5008 100p
VDD1V8_RF_G16
C5009 100p
VDD1V8_RF_D2
C5010 100p
VDD1V8_RF_C1
C5067 100p
VDD1V8_RF_PCIE_HSIC_A10
C5068 1u
C5069 10p
+3P3V_RADIO
VDD3V3_RF_M3
C5039 10u
C5015 100p
VDD3V3_RF_M9
C5018 10u
C5017 100p
VIO_RF_L12
C5019 0.1u
VDD3V3_RF_B11
C5040 1u
C5041 0.1u
+1P1V_INT_OUT
VDD11
C5029 0.1u
+3P3V_RADIO
T5008
C5020 0.1u
OPTION HOST VIO
R5039 DNP 0
R50117 0
VIO
C5030 0.1u
+1P1V_INT
1.1V
+1P1V_INT_OUT
R5042 0
+1P8V_INT
1.8V
+1P8V_INT_OUT
R5043 0
U5001A
VDD1V8_RF_PCIE_HSIC_A10
VDD1V8_RF_J1
VDD1V8_RF_K3
VDD1V8_RF_K9
VDD1V8_RF_K16
VDD1V8_RF_M14
VDD1V8_RF_C1
VDD1V8_RF_D2
VDD1V8_RF_NFC_E14
VDD1V8_RF_G1
VDD1V8_RF_F1
VDD1V8_RF_G16
VDD1V8_RF_H1
VDD1V8_RF_H16
VDD3V3_RF_B11
VDD3V3_RF_M3
VDD3V3_RF_M9
AVDD18_1
AVDD18_10
AVDD18_11
AVDD18_12
AVDD18_13
AVDD18_14
AVDD18_2
AVDD18_3
AVDD18_4
AVDD18_5
AVDD18_6
AVDD18_7
AVDD18_8
AVDD18_9
AVDD33_1
AVDD33_2
AVDD33_3
AVDD33_4
AVSS1
AVSS10
AVSS11
AVSS12
AVSS13
AVSS14
AVSS15
AVSS16
AVSS17
AVSS18
AVSS19
AVSS2
AVSS20
AVSS21
AVSS22
AVSS23
AVSS3
AVSS4
AVSS5
AVSS6
AVSS7
AVSS8
AVSS9
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
GPIO[6]
GPIO[7]
GPIO[8]/LED_OUT_WLAN
GPIO[9]/LED_OUT_BT
GPIO[10]/SER_WB
GPIO[11]/LED_OUT_NFC
GPIO[12]/PCIE_PERSTn
GPIO[13]/PCIE_W_DISABLE
GPIO[14]
GPIO[15]
GPIO[16]
GPIO[17]
GPIO[18]
GPIO[19]
GPIO[20]
GPIO[21]
GPIO[22]
GPIO[23]
GPIO[24]
CONFIG_HOST[0]
CONFIG_HOST[1]
CONFIG_HOST[2]
CONFIG_HOST[3]
BRF_ANT
BUCK11_SENSE
BUCK11_VOUT
BUCK18_SENSE
BUCK18_VOUT
WIFI_GPIO0
T5020
PCIE_WIFI_PERST_N [25]
PCIE_WIFI_DISABLE_N [25]
CONFIG_HOST[1]
BRF_ANT_M15
88W8897-B1-CBK2-T
R5071 DNP 49.9K
R5069 49.9K
R5068 49.9K
R5084 49.9K
R5067 49.9K
R5065 DNP 49.9K
R5064 DNP 49.9K
L5001 2.2uH
C5022 10u
L5002 2.2uH
C5023 10u
C5053 0.1u
C5054 0.1u
C5078 100p
Put C5078 close to pin C15
+3P3V_WWAN
L5008 FERRITE 30 Ohm
+3P3V_WWAN_ALT
C5049 0.1u
C5050 10u
C5042 0.1u
C5057 10p
WIFI > PCIe3
[20,33] PCIE_WIFI_CLKREQ_N
[20] PCIE_WIFI_RCLK_N
[20] PCIE_WIFI_RCLK_P
[24] PCIE_WIFI_TXN1
[24] PCIE_WIFI_TXP1
[24] PCIE_WIFI_RXN1
[24] PCIE_WIFI_RXP1
[25,33] PCIE_WIFI_WAKE_N
R5055 0
R5056 0
R5057 0
PCIE_WIFI_CLKREQ_N_R
PCIE_WIFI_RCLK_N_R
PCIE_WIFI_RCLK_P_R
C5072 0.1u PCIE_WIFI_TXN9_C
C5073 0.1u PCIE_WIFI_TXP9_C
C5070 0.1u PCIE_WIFI_RXN9_C
C5071 0.1u PCIE_WIFI_RXP9_C
T5009
[20,33] WLAN_PWD_N
T5019
R5046 49.9K DNP
C5026 0.1u DNP
C5063 0.1u
U5001B
PCIE_CLKREQn
PCIE_RCLK_N
PCIE_RCLK_P
PCIE_RX_N
PCIE_RX_P
PCIE_TX_N
PCIE_TX_P
PCIE_WAKEn
PDn
RES1
RES10
RES11
RES12
RES13
RES2
RES3
RES4
RES5
RES6
RES7
RES8
RES9
RF_CNTL0_N
RF_CNTL1_P
RF_TR_2_A
RF_TR_2_B
RF_TR_5_A
RF_TR_5_B
SD_CLK
SD_CMD
88W8897-B1-CBK2-T
T5002
T5003
T5005
T5004
WF_TCK
WF_TDI
WF_TDO
WF_TMS
R5079 49.9K
R5078 DNP 49.9K
BT -> USB2.0(5)
USB_DMNS
USB_DPLS
R5082 0
R5083 0
BT_USB_DN [24]
BT_USB_DP [24]
R5044 0
C5024 1u
C5025 10u
VBAT_IN
VBLDO33_CNTL
VBLDO33_SENSE
VDD11
VDD12
C5046 0.1u
VIO
VIO_RF
VIO_SD
VIO_RF_L12
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
XTAL_IN
XTAL_OUT
REF_CLK_IN
REF_CLK_OUT
R5085 0
SLP_CLK_IN
SER_DAT
SER_CSn
SER_CLK
R5077 49.9K
R5076 DNP 49.9K
SD_DAT[0]
SD_DAT[1]
SD_DAT[2]
SD_DAT[3]
X5002 FL4000023
U5005
GND1 5G_IN
ANT GND
GND3 2G_IN
LFD182G45MJ6D431
C5066 5.6p
C5034 22p
RF_TR_5_A
RF_TR_2_A
U5004
LFD182G45MJ6D431
C5064 5.6p
RF_TR_5_B
C5056 22p
RFIN_2_B
RF_CNTL1_P_V2
U5003
BGS12SN6
VDD
RFIN
CTRL
GND
RF1
RF2
RFV1_2_B
RFV2_2_B
C5035 22p
C5036 5.6p
RF_TR_2_B
BRF_ANT_M15
+3P3V_RADIO
R5014 51K
R5016 51K DNP
T5021
R5013 0
RF_CNTL1_P
RF_CNTL0_N
C5038 10p
C5037 10p
R5015 51K DNP
R5017 51K
EEPROM
U5002
AT24C16C
R5048 10K
R5047 10K
C5033 0.1u
T5024
T5025
SER_CLK
SER_DAT
AT24C16C-SSHM-B bulk packaging 0502-00P40QS
AT24C16C-SSHM-T Tape & Reel 0502-00CT0QS
Title: Wi-Fi_BT
<OrgName>
<OrgAddr1>
Engineer:
Size A2
Project Name CHARIOT
Rev 1.00
Date: Thursday, August 03, 2017
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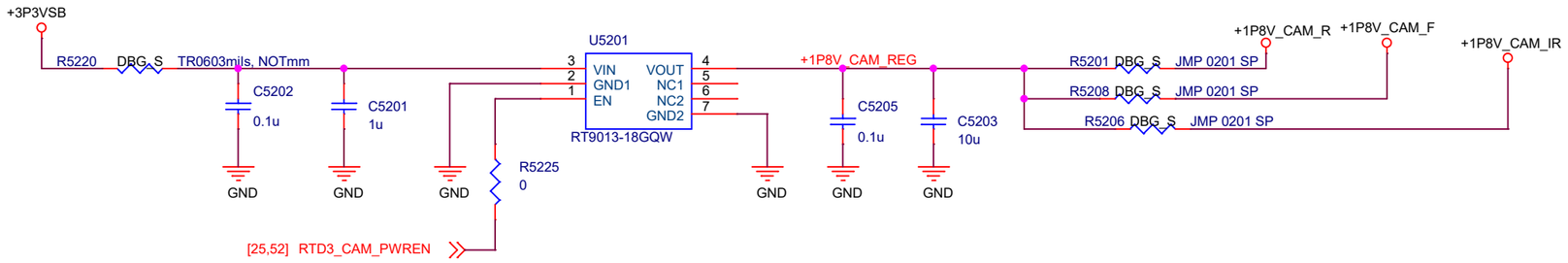
Title:	X				
<OrgName>	Engineer:			<OrgAddr1>	
Size: A2	Project Name: CHARIOT				Rev: 1.00
Date: Thursday, August 03, 2017		Sheet 51 of 76			

IR IDD-IO: Typ: 40mA Max: 55mA

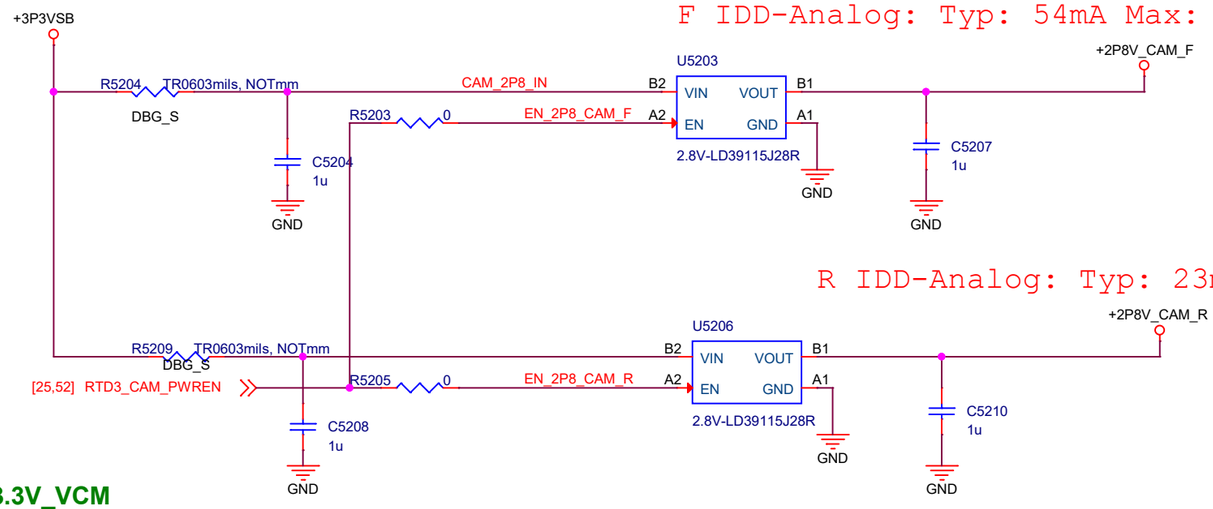
Front IDD-IO+Core: Typ: 67.5mA Max: 93mA

Rear IDD-IO: Typ: 3.3mA Max: 4.5mA

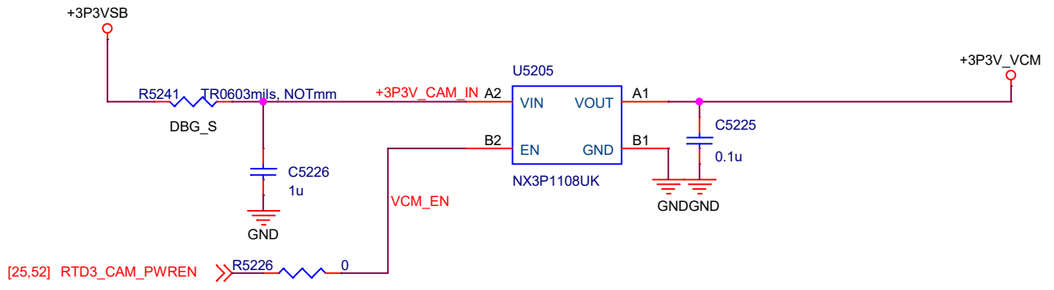


2V8_LDO_Voltage Regulator

F IDD-Analog: Typ: 54mA Max: 70mA

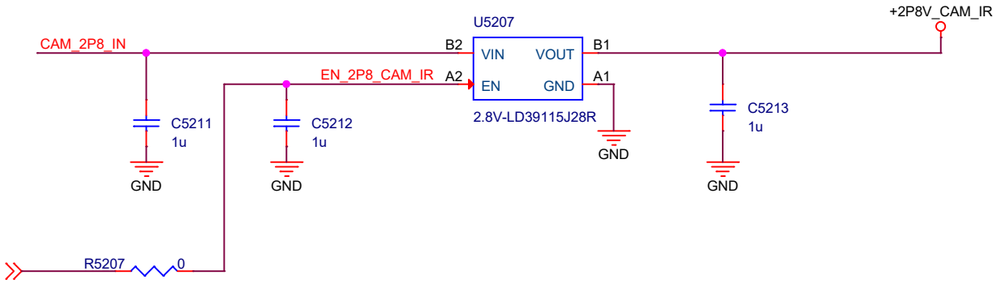


R IDD-Analog: Typ: 23mA Max: 30mA

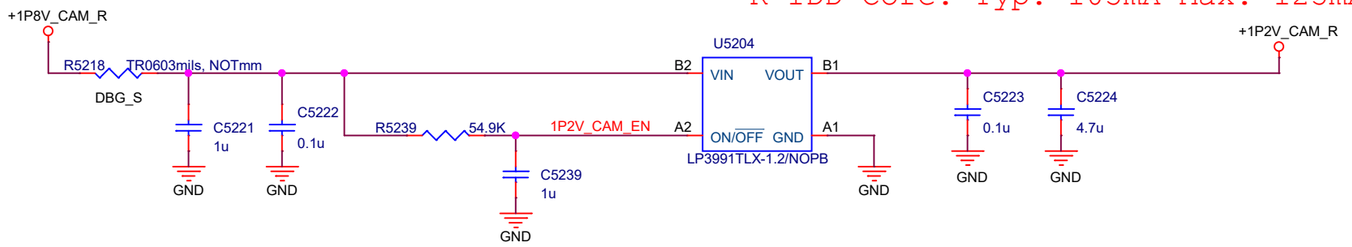


+3.3V_VCM
Imax=0.5A
07132016

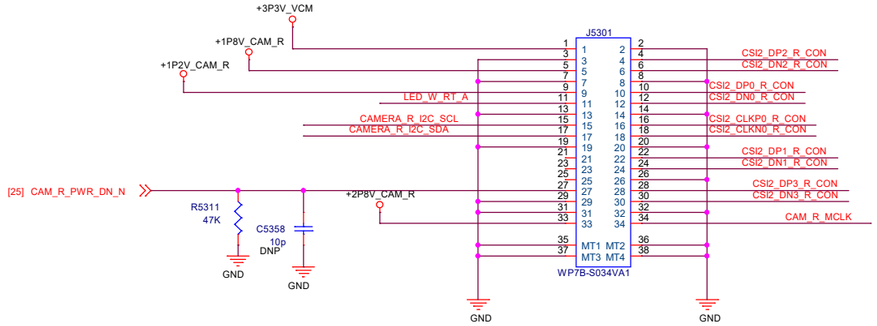
IR IDD-Analog: Typ: 16mA Max: 20mA

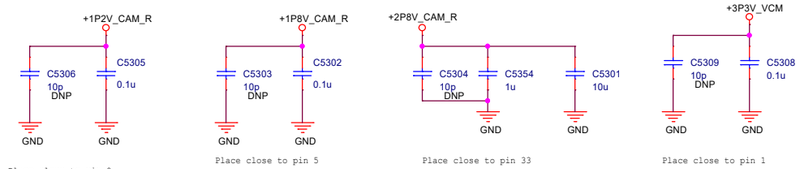


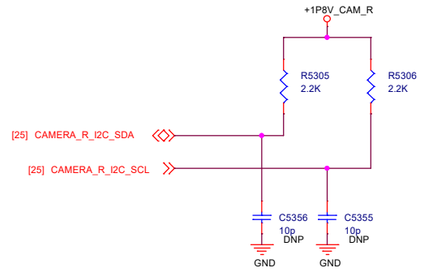
R IDD-Core: Typ: 105mA Max: 125mA



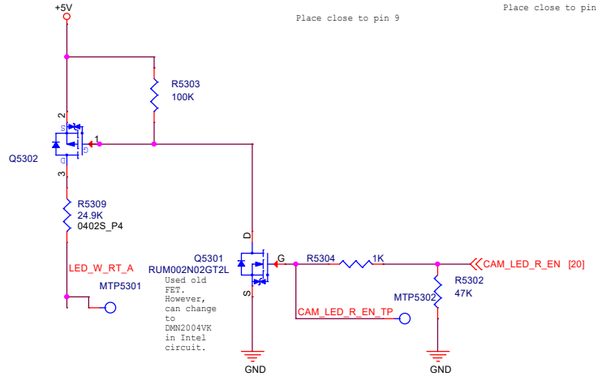
Title:	Camera power		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 52 of 76		

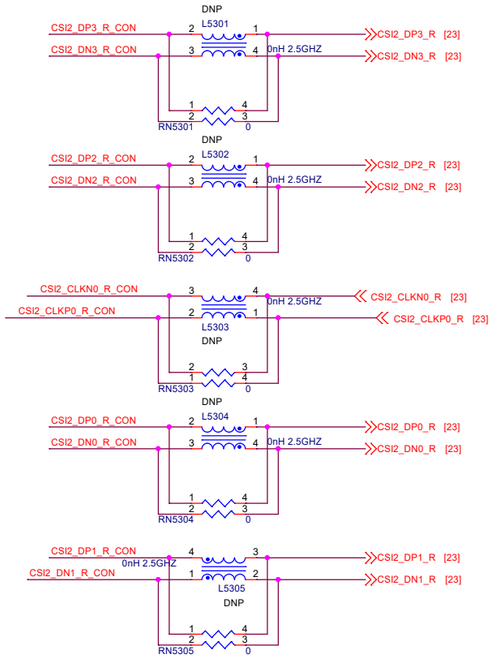


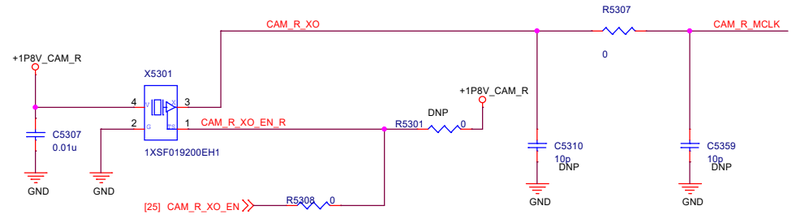




7-bit I2C Address = 0x20 Sensor
7-bit I2C Address = 0x18 VCM

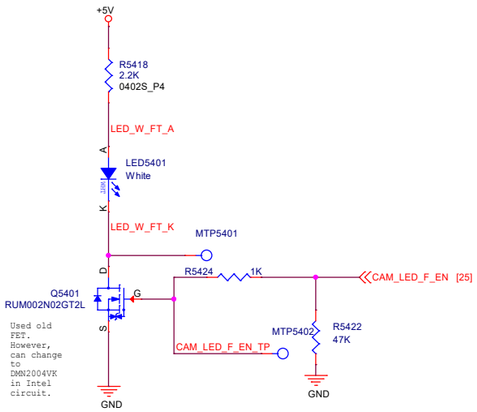


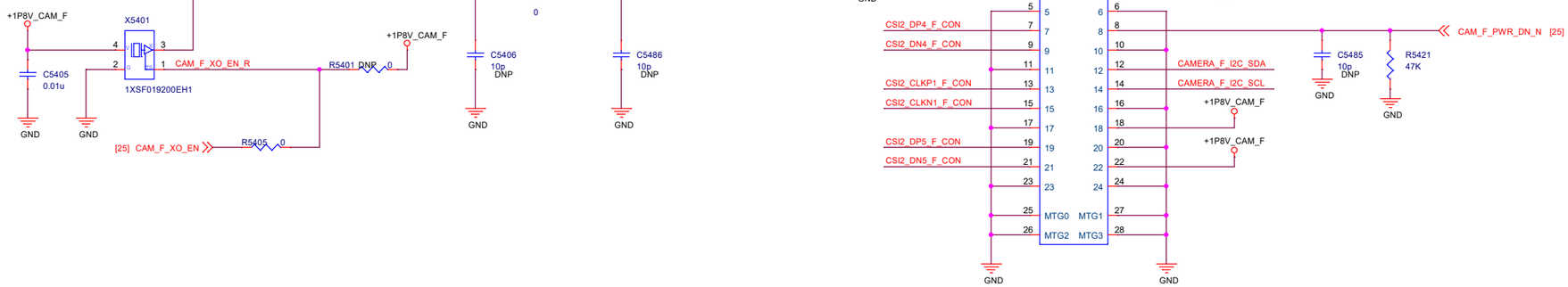




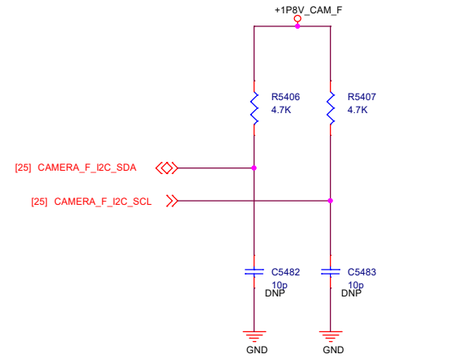
7-bit I2C Address = 0x10 Sensor
7-bit I2C Address = 0x0C VCM

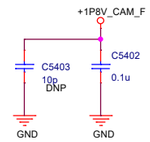
Title:	Camera Rear		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 53 of 76		



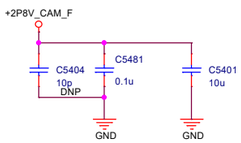


7-bit I2C Address = 0X36

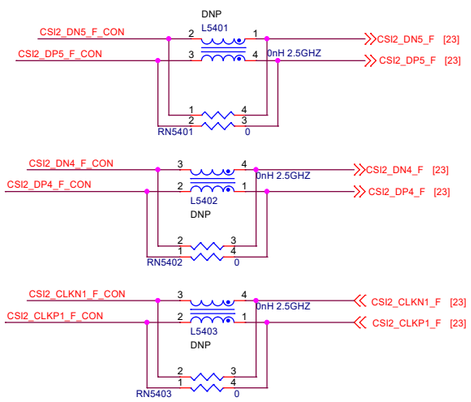




Place close to pin 18 and 22



Place close to pin 4



Title:	Camera Front		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 54 of 76		

PIN17=PIN2*PIN4*PIN3*PIN6
PIN8=PIN12*PIN6
PIN9=PIN5*PIN6

VDD_BATA_PACK
D5501 RB520CS3002L
DNP
+6VA_15VA
+VSYS
D5504 RB520CS3002L

U5505 74AUP1G07GX
[10] H_THERMTRIP#
+VCCST_CPU
+3P3V
R5517 4.7K
C5503 0.1u
GND

T5505
[34,61,62,64,65] SLP_S3_DRV#
[34,61] ALL_SUS_PWRGD
[56] +VCCIO_PWRGD
[34,66] VRM_PWRGD
[60,61] +1P2V_DUAL_PWRGD
[22,34] SLP_S3#
[22,33,34,38,43,73] PLT_RST#_BUF
[30,35] PWRBTN#
[35] PCH_PWROK_SAM
[39] DEVICE_RST#
R5506 0
R5507 0
R5508 0
R5509 0
R5510 0
R5511 0
R5561 0
R5560 0
T5507 T5515 T5512 T5506 T5511 T5514 T5503 T5501 T5509

U5504 SLG4U41281VTR
SPL_3_DRV# SUS_PGD IO_PGD VRM_PGD 1P2V_PGD SLP_3# THERMTRIP# PLT_RST# START# PCH_PWROK_SAM RST#
VDD VCORE_EN FORCE_OFF# P_B# MCU_PWR_CTRL S_DBG-MCU_DBG EN_VCCIO PCH_PWROK_PCH GND

+3P3VAS
C5520 0.1u
GND
T5510 R5512 0 VCORE_EN [66]
T5504 R5516 0 FORCE_OFF# [36]
T5508 D5502 K A RB520CS3002L SYS_HW_RST# [71]
R5573 100K DNP
R5574 DBG_D 0 DBG_SAM_FLASH_EN [31,71]
T5516 T5513
EN_VCCIO [56]
T5517 PCH_PWROK_PCH [22]

U5506 74AUP1G07GX
+3P3VSB
C5533 0.1u
+VCCST_CPU
R5572 1K
VCCST_PWRGD [22]
T5518

+6VA_12VA
Iin= A
Trace Width>30mil

+6VA_15VA
PTP5506 PTP5505
R5521 SENS LOAD NO-MSPN-00310 DBG_S
C5509 10u
R5532 10K
3P3VAS_EN

U5501 MP2269GD-Z
VIN1 MODE EN PG BIAS VCC NC AGND PGND-8 PGND-3
SW BST FB FRQ SS
+3P3VAS_VIN
R5501 DNP 1K
+3P3VAS_SW L5501 6.8uH +3P3VAS_REG
R5531 DBG_STR0603mls_NOTmm PTP5504
C5514 1u
+3P3VAS_BST
C5504 5.6p
R5535 1M
+3P3VAS_FB
R5515 324K
C5505 22u
C5521 22u PTP5503
+3P3VAS_VCC
+3P3VAS_FREQ
+3P3VAS_SS
C5519 1u 0201 10V
C5515 0.012u
R5533 165K
3P3VA_GND
GND

+3P3VAS
C5501 1u
U5502 NX3P1108UK
VIN VOUT EN GND A1 A2 B1 B2
+3P3VA_REG
R5513 DBG_STR0603mls_NOTmm PTP5507
PTP5508
C5502 0.1u
+3P3VA
R5505 10K
3P3VA_EN
T5502

+3P3VA
Imax=0.1A
07132016

MODE
FLOAT PFM/PWM
PU PWM

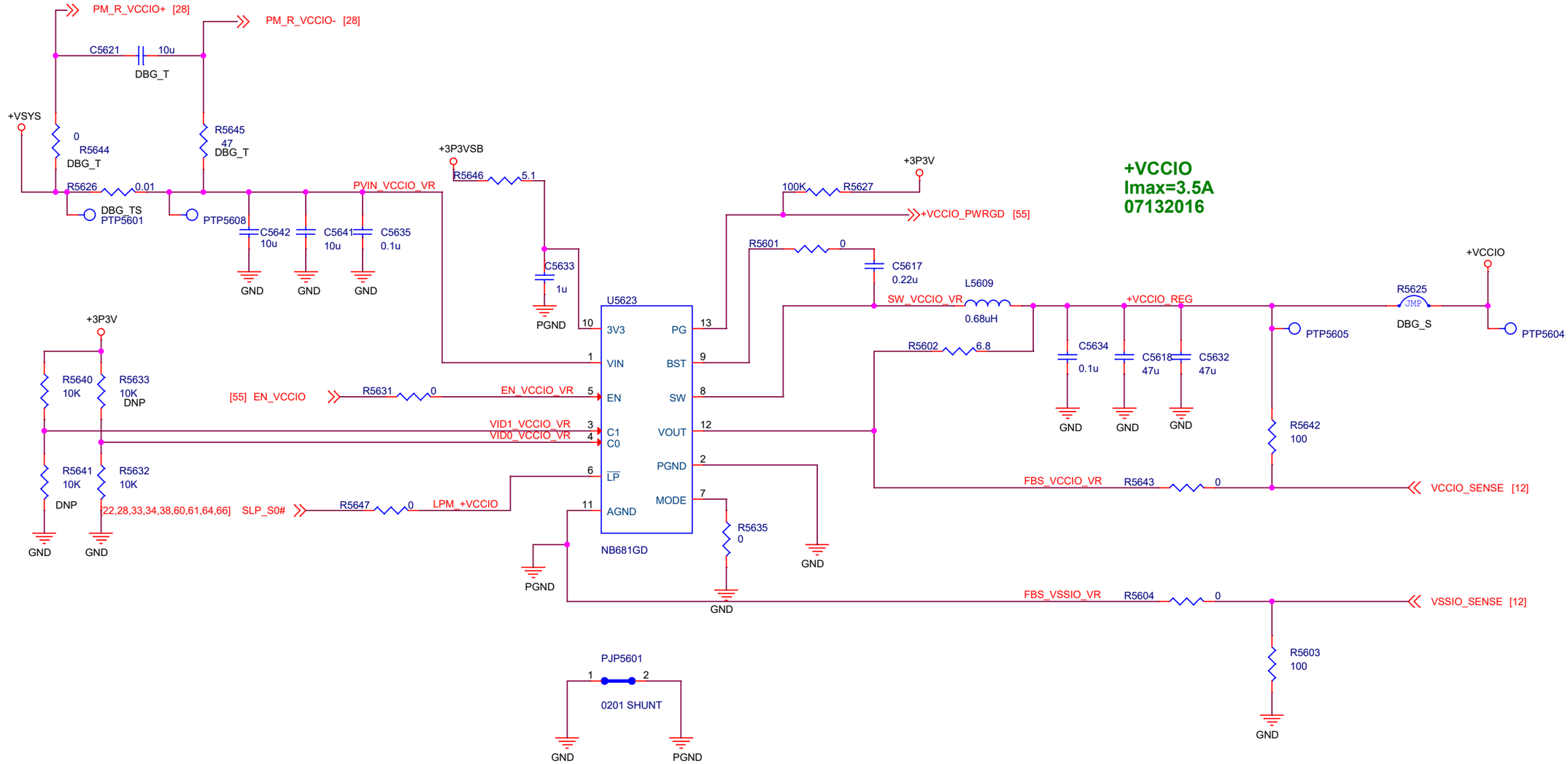
R5502 0201 SHUNT
3P3VA_GND
GND

fs = 86500/(R+6.5)
500KHz

PWR_SL1_F
PWR_SL1_F_S
D5503 RB520CS3002L
Q5505
+6VA_15VA
R5546 249K
C5532 0.01u
PWR_SL1_F_S_DRI
R5545 499K
SL1_PWR_GOOD#
[70] SL1_PWR_GOOD
R5547 249K
C5531 0.1u DNP
Q5506 RUM002N02GT2L

+3P3VAS
R5569 1.5K
D5505 RB520CS3002L
D5506 RB520CS3002L
+VCC_RTC
R5514 47K DNP
[34] VCCRTC_RST
R5570 1% 499 VCCRTC_RST_R
R5571 100K
RUM002N02GT2L Q5507

Title:	3P3VA & BKL PWR		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 55 of 78		



Title:	+VCCIO	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
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[1/7] Change M57L1, M57L2, M57L3, M57L4 and M57L5 to 0R

[10] EDP_AUXN — C5724 0.1u — EDP_AUXN_C — L5701 (DLP11TB800UL2L) — EDP_AUXN_R
[10] EDP_AUXP — C5725 0.1u — EDP_AUXP_C — L5701 (DLP11TB800UL2L) — EDP_AUXP_R
L5701 DNP
RN5701 0

[10] EDP_TXN0 — C5720 0.1u — EDP_TXN0_C — L5702 (DLP11TB800UL2L) — EDP_TXN0_R
[10] EDP_TXP0 — C5721 0.1u — EDP_TXP0_C — L5702 (DLP11TB800UL2L) — EDP_TXP0_R
L5702 DNP
RN5702 0

[10] EDP_TXN1 — C5722 0.1u — EDP_TXN1_C — L5703 (DLP11TB800UL2L) — EDP_TXN1_R
[10] EDP_TXP1 — C5723 0.1u — EDP_TXP1_C — L5703 (DLP11TB800UL2L) — EDP_TXP1_R
L5703 DNP
RN5703 0

[10] EDP_TXN2 — C5726 0.1u — EDP_TXN2_C — L5704 (DLP11TB800UL2L) — EDP_TXN2_R
[10] EDP_TXP2 — C5727 0.1u — EDP_TXP2_C — L5704 (DLP11TB800UL2L) — EDP_TXP2_R
L5704 DNP
RN5704 0

[10] EDP_TXN3 — C5728 0.1u — EDP_TXN3_C — L5705 (DLP11TB800UL2L) — EDP_TXN3_R
[10] EDP_TXP3 — C5729 0.1u — EDP_TXP3_C — L5705 (DLP11TB800UL2L) — EDP_TXP3_R
L5705 DNP
RN5705 0

+1P8V_PANEL, +3P3V_PANEL
R5701 4.7K
R5702 4.7K
J5701
[25,33] PANEL_I2C_SDA — T5711
PANEL_I2C_SCL [25,33] — T5710
PTP5705
PTP5706
GND
T5701 — PANEL_INT [25,33]
TCON_TDI — PTP5701
TCON_TMS — PTP5702
TCON_TCK — PTP5703
TCON_TDO — PTP5704 — TCON_VENDOR_ID [20]
EDP_HPD [10]
PANEL_BIST — T5712
PANEL_LOGO_CON
PANEL_VSYNCH — T5713 — PANEL_VSYNCH [30]
PANEL_TS_SPI_CS [30]
PANEL_TS_INTn [30]
PANEL_TS_SPI_MISO [30]
PANEL_TS_SPI_CLK [30]
EDP_TXN0_R, EDP_TXP0_R, EDP_TXN1_R, EDP_TXP1_R, EDP_TXN2_R, EDP_TXP2_R, EDP_TXN3_R, EDP_TXP3_R, EDP_AUXN_R, EDP_AUXP_R
[72,76] BKLT_FB8, BKLT_FB6, BKLT_FB4, BKLT_FB2
BKLT_FB7 [72,76], BKLT_FB5 [72,76], BKLT_FB3 [72,76], BKLT_FB1 [72,76]
+VCC_EDP_BKLT_OUT
MT1 MT2 MT3 MT4
GND

PANEL_BIST — R5705 100K — GND

+3P3VSB, +1P8V_PANEL
U5701 74AUP1G07GX
VCC, I, O, NC1, GND
[35] PANEL_LOGO
PANEL_LOGO_CON
R5704 4.7K
C5715 0.1u
GND

T5714
EDP_HPD
TCON_VENDOR_ID
C5713 0.1u DNP — GND
C5718 0.1u DNP — GND

+3P3V_PANEL — C5704 0.47u — GND
+3P3V_PANEL — C5701 1u — GND
+3P3V_PANEL — C5712 0.1u — GND

+VCC_EDP_BKLT_OUT
C5705 0.47u — GND
C5706 2.2u 50V — GND
C5711 0.1u — GND
C5730 2.2u 50V — GND

Title:	eDP connector		
<OrgName>	Engineer:	<OrgAddr1>	
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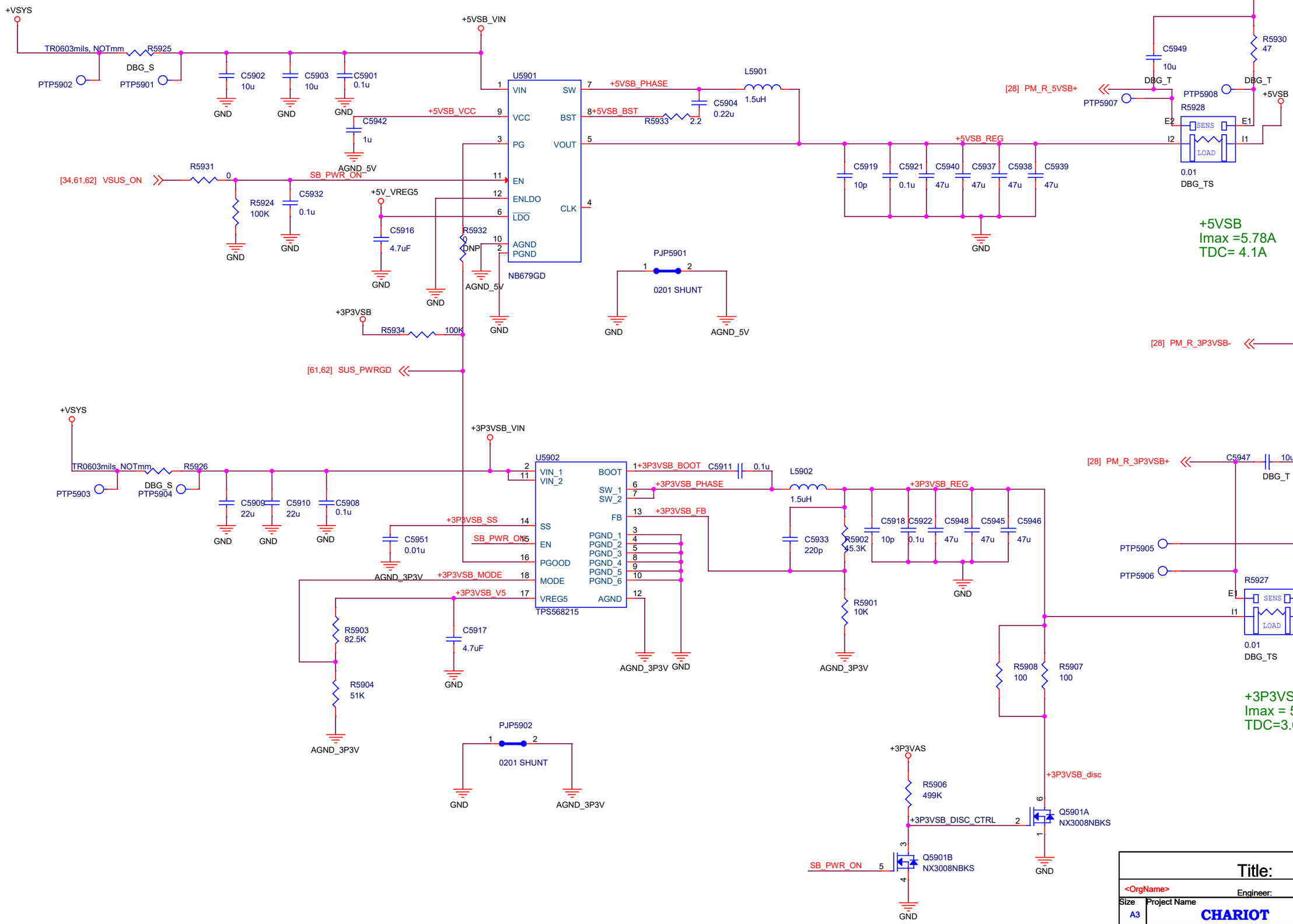
Title: X				
<OrgName>	Engineer:		<OrgAddr1>	
Size A3	Project Name CHARIOT			Rev 1.00
Date: Thursday, August 03, 2017		Sheet 58 of 76		


+VSYS
TR0603mils_NOTmm
R5925
DBG_S
PTP5902
PTP5901
C5902
10u
C5903
10u
C5901
0.1u
GND
+5VSB_VIN
U5901
VIN
SW
BST
VCC
PG
VOUT
EN
ENLDO
LDO
CLK
AGND
PGND
NB679GD
1
7
8
9
3
5
11
12
6
4
10
2
+5VSB_PHASE
+5VSB_BST
+5VSB_VCC
L5901
1.5uH
C5904
0.22u
R5933
2.2
C5942
1u
AGND_5V
R5931
0
SB_PWR_ON
[34,61,62] VSUS_ON
R5924
100K
C5932
0.1u
+5V_VREG5
C5916
4.7uF
R5932
0
DNP
PJP5901
0201 SHUNT
+5VSB_REG
C5919
10p
C5921
0.1u
C5940
47u
C5937
47u
C5938
47u
C5939
47u
[28] PM_R_5VSB-
[28] PM_R_5VSB+
C5949
10u
DBG_T
R5930
47
PTP5907
PTP5908
R5928
SENS
LOAD
E2
E1
I2
I1
0.01
DBG_TS
+5VSB
Imax =5.78A
TDC= 4.1A
+3P3VSB
R5934
100K
[61,62] SUS_PWRGD
+3P3VSB_VIN
U5902
VIN_1
VIN_2
BOOT
SW_1
SW_2
FB
SS
EN
PGOOD
MODE
VREG5
PGND_1
PGND_2
PGND_3
PGND_4
PGND_5
PGND_6
AGND
TPS568215
+3P3VSB_BOOT
C5911
0.1u
+3P3VSB_PHASE
+3P3VSB_FB
+3P3VSB_SS
SB_PWR_ON
+3P3VSB_MODE
+3P3VSB_V5
C5951
0.01u
AGND_3P3V
L5902
1.5uH
C5933
220p
R5902
45.3K
R5901
10K
C5918
10p
C5922
0.1u
C5948
47u
C5945
47u
C5946
47u
+3P3VSB_REG
R5903
82.5K
R5904
51K
C5917
4.7uF
PJP5902
0201 SHUNT
[28] PM_R_3P3VSB-
[28] PM_R_3P3VSB+
C5947
10u
DBG_T
R5929
47
PTP5905
PTP5906
R5927
SENS
LOAD
E1
E2
I1
I2
0.01
DBG_TS
+3P3VSB
Imax = 5.15A
TDC=3.61A
R5908
100
R5907
100
+3P3VAS
R5906
499K
+3P3VSB_DISC_CTRL
+3P3VSB_disc
Q5901A
NX3008NBKS
Q5901B
NX3008NBKS
SB_PWR_ON
Title:
+5VSB & +3P3VSB
<OrgName>
Engineer:
<OrgAddr1>
Size
A3
Project Name
CHARIOT
Rev
1.00
Date:
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76

+VSYS
Iin=1.7A
Trace Width>80mil

+VSYS
TR0603mils, NOTmm R6019
PTP6002
DBG_S
PTP6001
C6018 10u
C6017 10u
+1P2V_DUAL_VIN
C6019 0.1u
GND

+3P3VSB
R6003 5.1
C6002 1u
1P2DUAL_GND
+1P2V_DUAL_3V3

Low power mode for Connected Stanby
[55,61] +1P2V_DUAL_PWRGD
[11] DDR_PG_CTRL
[22,28,33,34,38,56,61,64,66] SLP_S0#
R6015 100K
R6024 0
R6025 DNP 0
+1P2V_DUAL_LP

U6002
NB685A
1 VIN
3 3V3
4 AGND
12 PG
16 EN1
15 EN2
11 OTW#
14 MODE
2 PGND
10 BST
9 SW
13 FB
6 VDDQ
5 VTT
8 VTTS
7 VTTREF

R6002 0 +1P2V_DUAL_BOOT_R
C6001 0.1u
L6001 0.47uH
+1P2V_DUAL_REG
+1P2V_DUAL_PHASE
+1P2V_DUAL_FB
R6026 DNP 1M
C6015 220p
R6011 499
R6014 40.2K
R6013 40.2K
C6021 10p
C6009 0.1u
C6027 47u
C6014 47u
C6012 47u

+1P2V_DUAL
Imax = 6.14A
TDC=4.76A
07132016

PTP6003
PTP6004
+1P2V_DUAL
R6020 JMP
DBG_S

U6004
74AUP1G08GX
[22,34] SLP_S4#
[34,61,62] SLP_S4_DRV#
VCC
GND
C6028 0.1u
+1P2V_DUAL_EN
C6003 0.01u

+1P2V_DUAL_MD
R6009 0

+VDDQ_VREF
C6016 0.22u

+V_VDDQ_VTT
Imax=0.6A
Trace Width>40mil
07132016

VTTSNS_VDDQ_VTT_REG
R6023 TR0603mils, NOTmm
DBG_S
PTP6005
PTP6006
+V_VDDQ_VTT
C6005 10u
C6007 10u

PJP6002
2 1
0201 SHUNT
1P2DUAL_GND

+VCCPLL_OC
Imax=0.13A
Trace Width>40mil
07132016

+5VSB
+1P2V_DUAL
U6003
SLG5NT1533V
1 VDD
2 ON
3-4 D1-D2
S1-S2 5-6
CAP 7
GND 8
+VCCPLL_OC_CAP
+VCCPLL_OC_REG
+VCCPLL_OC
R6028 TR0603mils, NOTmm
DBG_S
PTP6007
PTP6008
C6022 0.1u
C6025 10u
C6026 470p
C6023 1u
C6024 10u DNP
[61] S0iX_EN
R6029 0

Title:	+1P2V_DUAL&+VTT		
<OrgName>	Engineer:	<OrgAddr1>	
Size A3	Project Name CHARIOT		Rev 1.00
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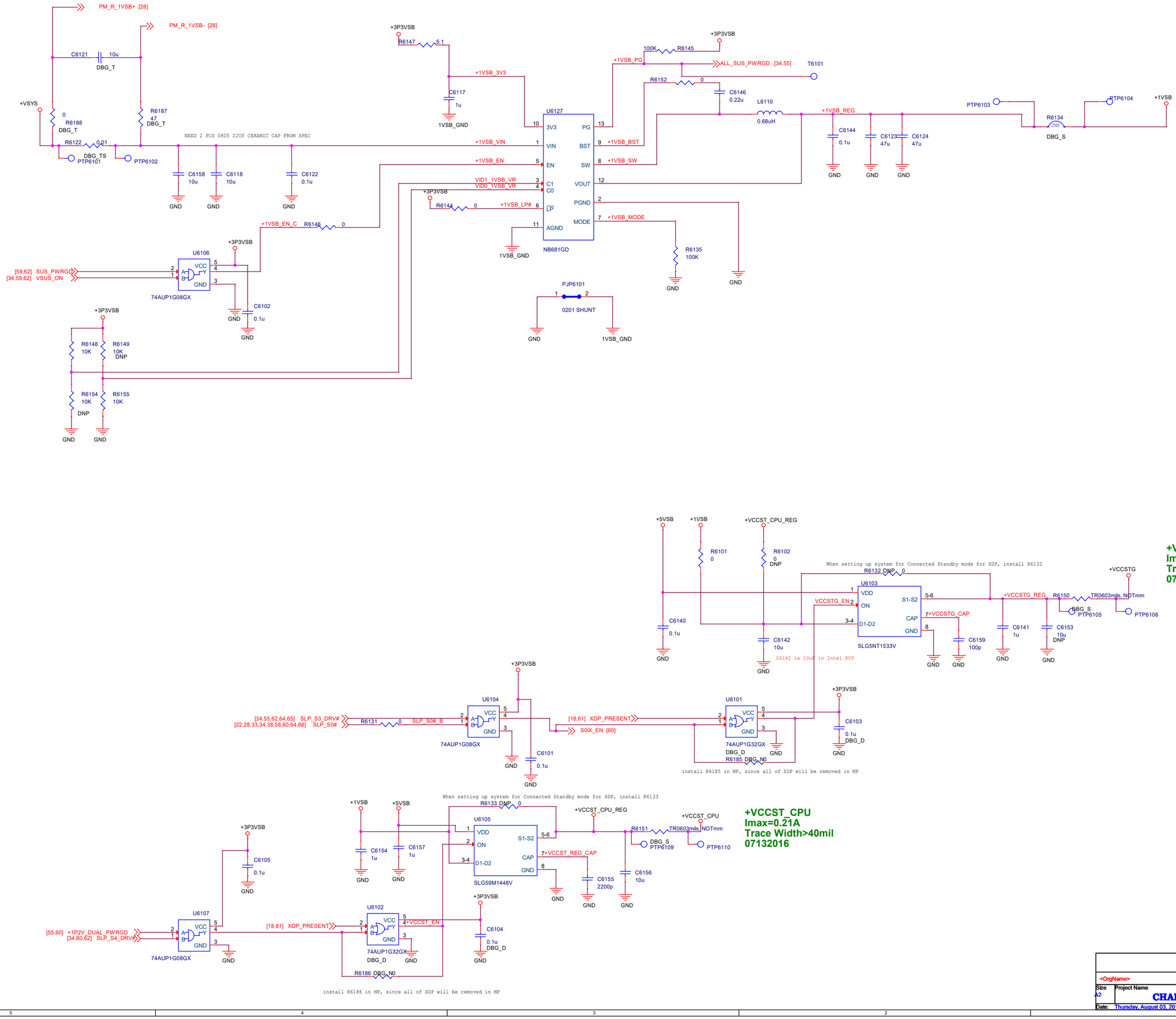
PM_R_1VSB+ [28]
PM_R_1VSB- [28]
C6121 10u DBG_T
+VSYS
R6188 0 DBG_T
R6187 47 DBG_T
R6122 0.01 DBG_TS
PTP6101
PTP6102
NEED 2 PCS 0805 22Uf CERAMIC CAP FROM SPEC
C6158 10u
C6118 10u
C6122 0.1u
GND
+3P3VSB
R6147 5.1
C6117 1u
1VSB_GND
+1VSB_3V3
U6127
NB681GD
3V3
VIN
EN
C1
C0
LP
AGND
PG
BST
SW
VOUT
PGND
MODE
+1VSB_VIN
+1VSB_EN
VID1_1VSB_VR
VID0_1VSB_VR
+1VSB_LP#
+1VSB_PG
+1VSB_BST
+1VSB_SW
+1VSB_MODE
100K R6145
ALL_SUS_PWRGD [34,55]
T6101
R6152 0
C6146 0.22u
L6110 0.68uH
+1VSB_REG
C6144 0.1u
C6123 47u
C6124 47u
PTP6103
R6134 0MF DBG_S
PTP6104
+1VSB
R6135 100K
PJP6101
0201 SHUNT
+1VSB_EN_C R6146 0
U6106
74AUP1G08GX
[59,62] SUS_PWRGD
[34,59,62] VSUS_ON
C6102 0.1u
R6148 10K
R6149 10K DNP
R6154 10K DNP
R6155 10K
+VCCSTG
Imax=0.02A
Trace Width>40mil
07132016
+5VSB
+VCCST_CPU_REG
R6101 0
R6102 0 DNP
When setting up system for Connected Standby mode for XDP, install R6132
R6132 DNP 0
U6103
SLG5NT1533V
VDD
ON
D1-D2
S1-S2
CAP
VCCSTG_EN
+VCCSTG_CAP
+VCCSTG_REG
R6150 TR0603mils, NOTmm
DBG_S PTP6105
PTP6106
C6140 0.1u
C6142 10u
C6142 is 10uf in Intel RVP
C6159 100p
C6141 1u
C6153 10u DNP
[34,55,62,64,65] SLP_S3_DRV#
[22,28,33,34,38,56,60,64,66] SLP_S4#
R6131 0 SLP_S0# B
U6104
U6101
74AUP1G08GX
74AUP1G32GX
[18,61] XDP_PRESENT
S0IX_EN [60]
C6101 0.1u
C6103 0.1u DBG_D
R6185 DBG_N0
install R6185 in MP, since all of XDP will be removed in MP
When setting up system for Connected Standby mode for XDP, install R6133
R6133 DNP 0
U6105
SLG59M1448V
C6154 1u
C6157 1u
C6105 0.1u
C6155 2200p
C6156 10u
R6151 TR0603mils, NOTmm
DBG_S PTP6109
PTP6110
+VCCST_CPU
Imax=0.21A
Trace Width>40mil
07132016
U6107
U6102
[55,60] +1P2V_DUAL_PWRGD
[34,60,62] SLP_S4_DRV#
[18,61] XDP_PRESENT
+VCCST_EN
C6104 0.1u DBG_D
R6186 DBG_N0
install R6186 in MP, since all of XDP will be removed in MP
Title: +1VSB
<OrgName>
Engineer:
<OrgAddr1>
Size A2
Project Name CHARIOT
Rev 1.00
Date: Thursday, August 03, 2017
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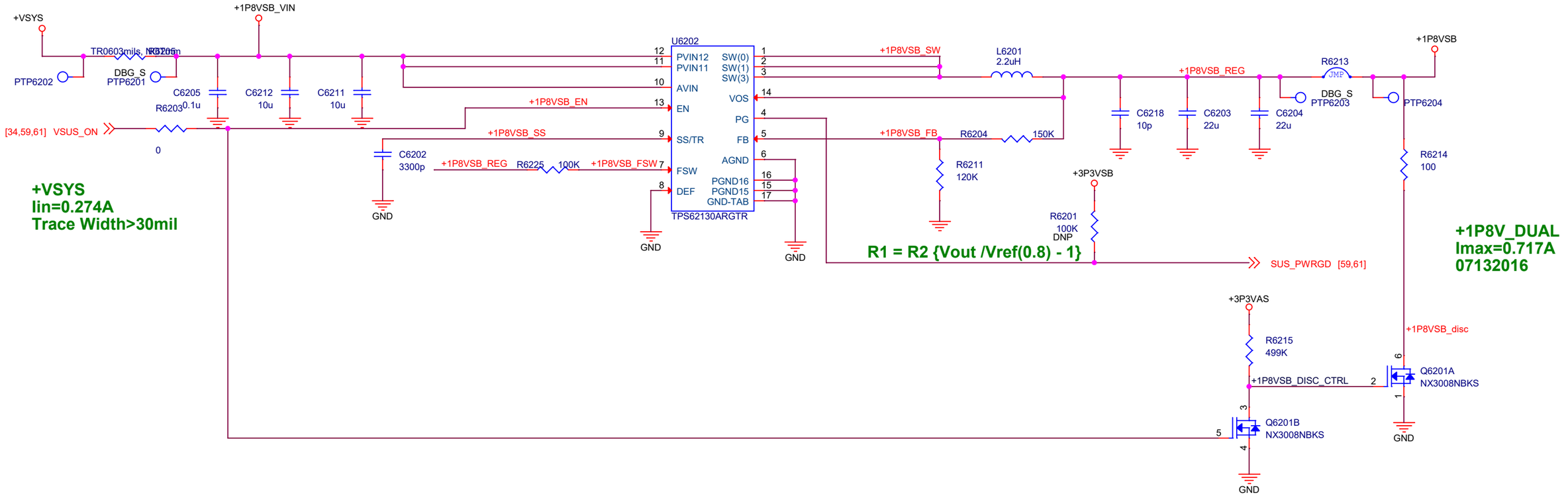

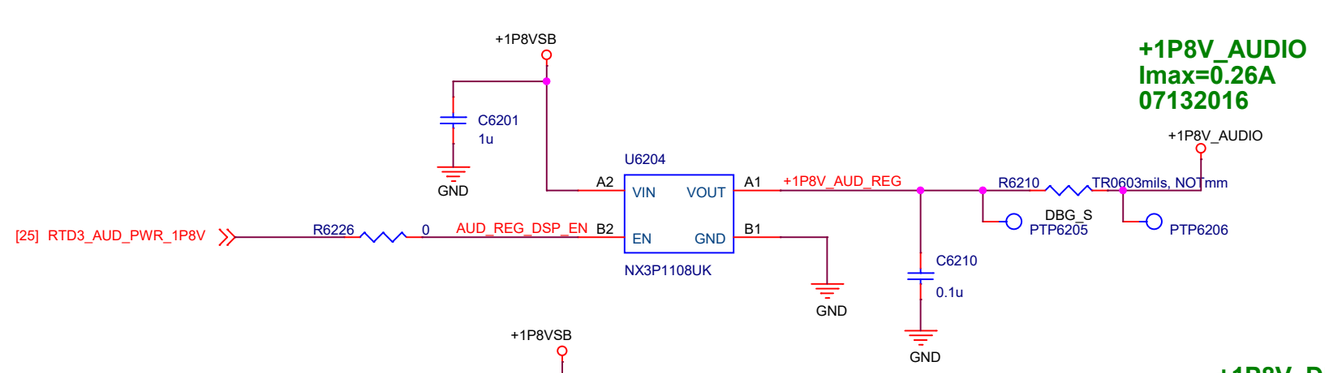

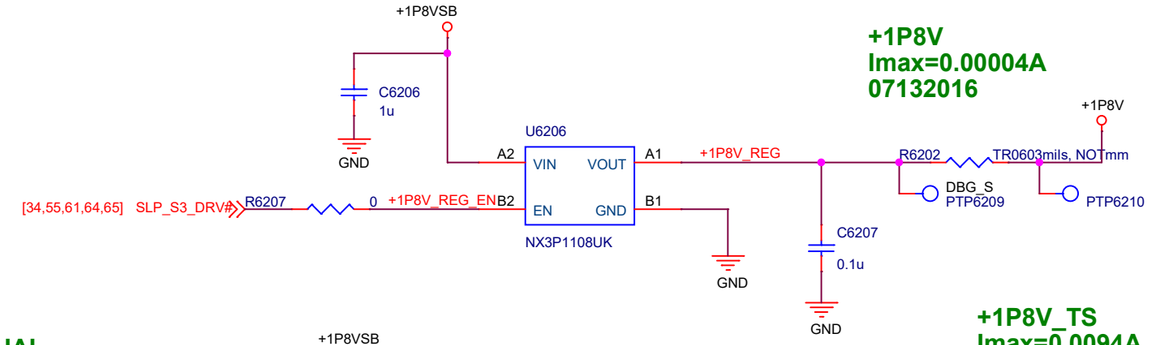

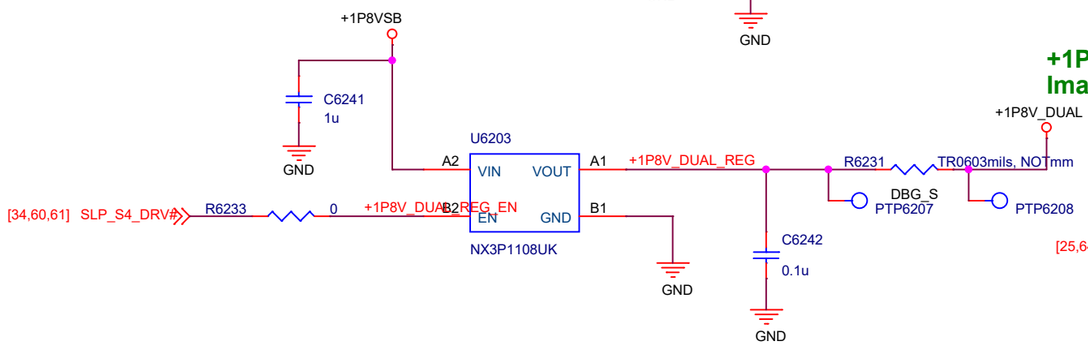

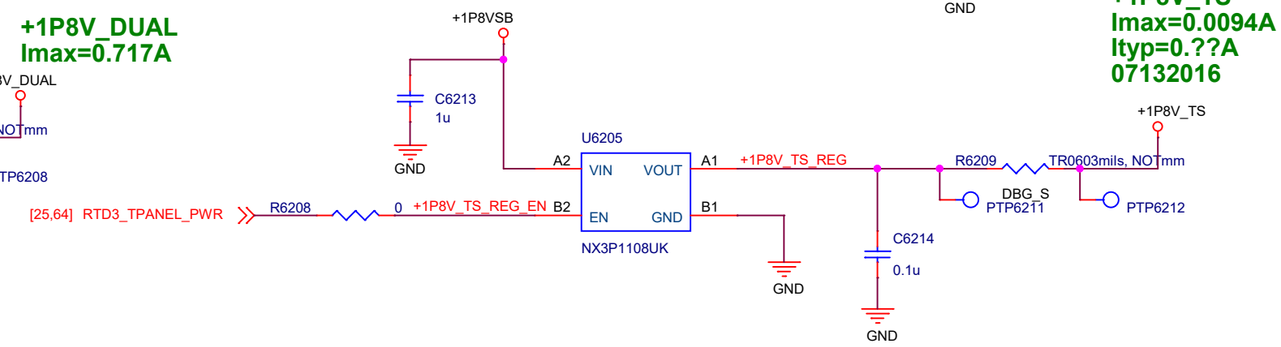

Title:	+1.8VSB & Load SW		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
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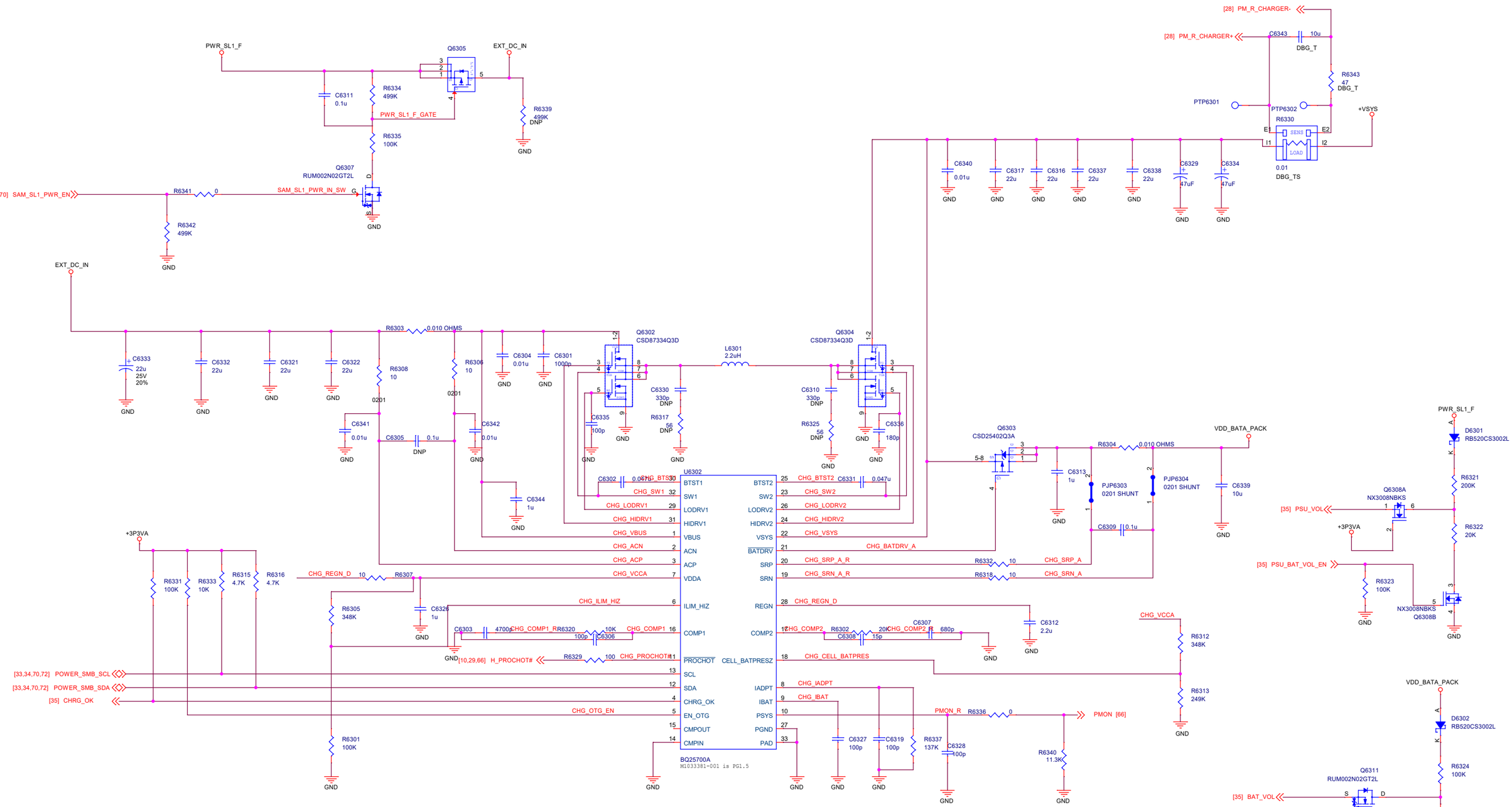
+VSYS: 6V(TBD) to 8.75V



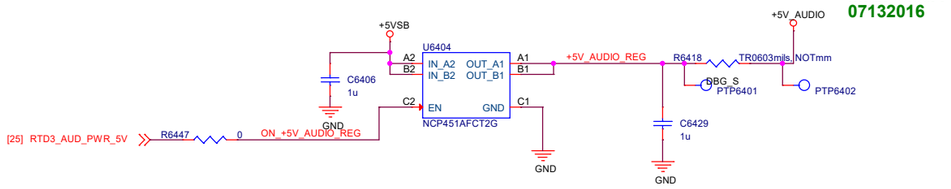
in PG1.2, OTG is active high

ILIM_HIZ current limit equation - (VILIM_HIZ ?1 V) / 40 = ACP - ACN

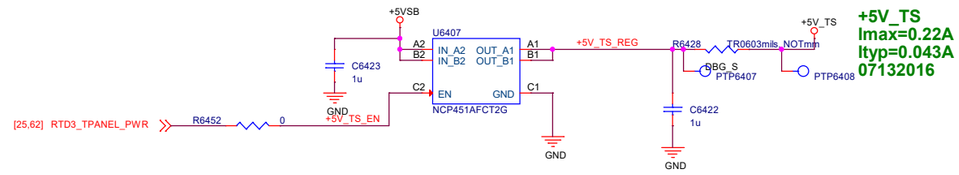
7-bit I2C Address = 0x09

Title:	CHARGER		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 63 of 76		

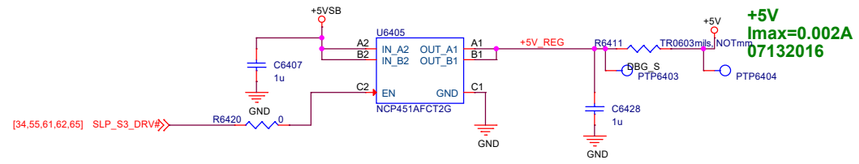
+5V_AUDIO
Imax=0.05A
07132016



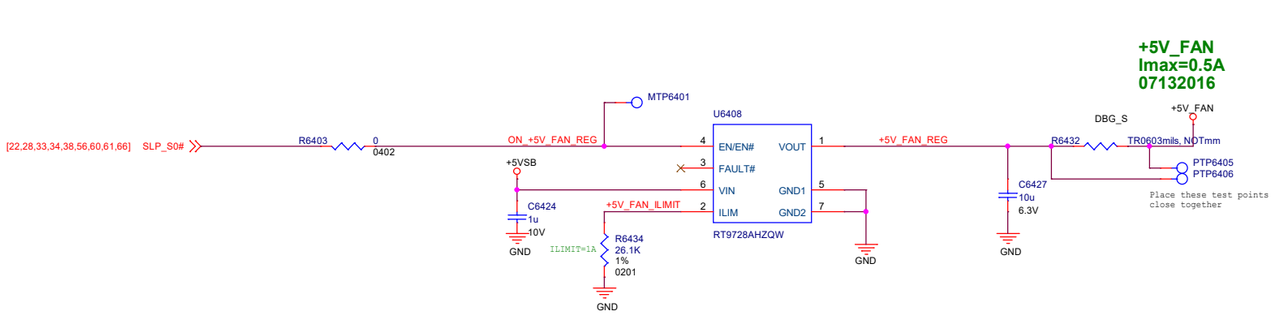
+5V_TS
Imax=0.22A
Ityp=0.043A
07132016



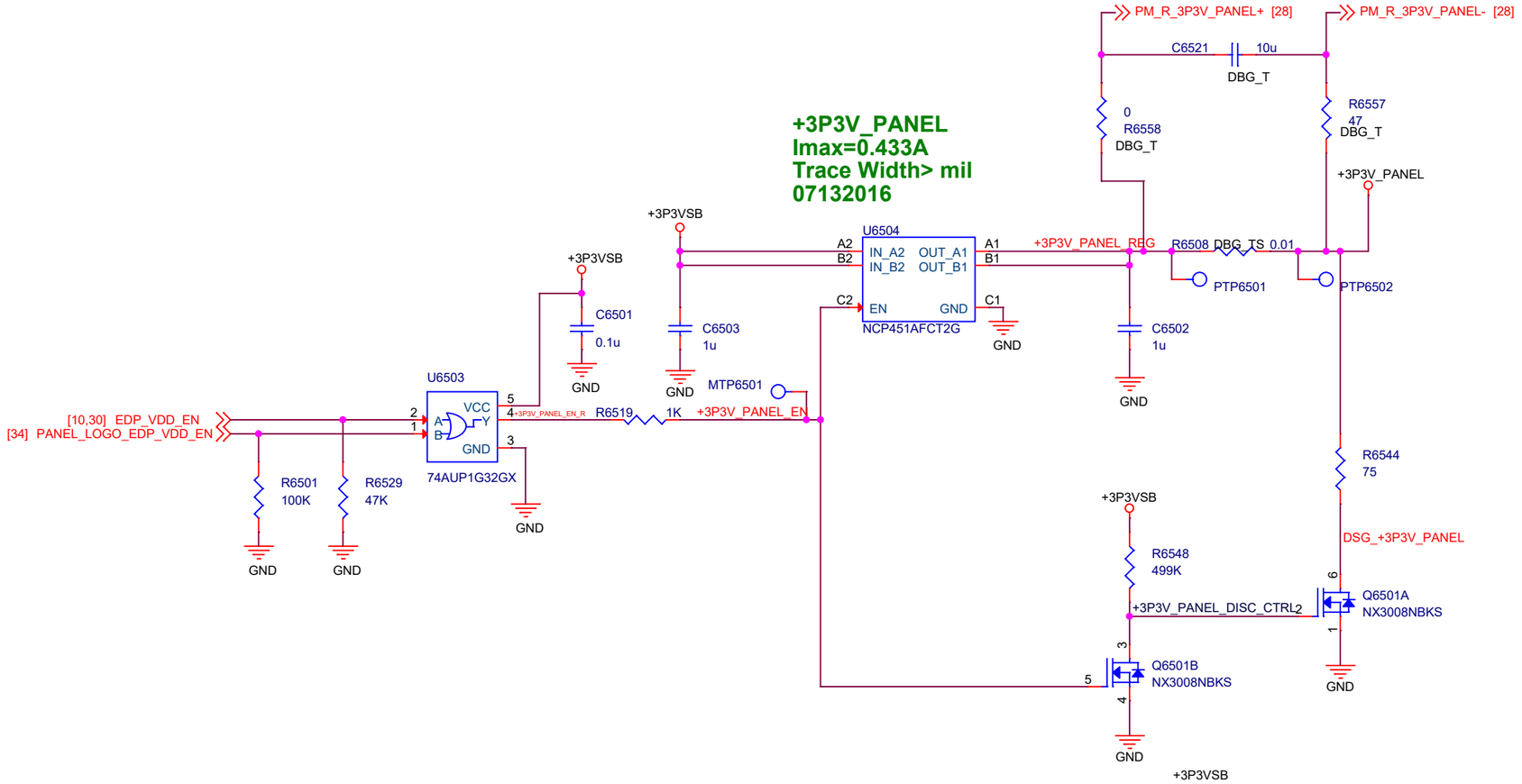
+5V
Imax=0.002A
07132016



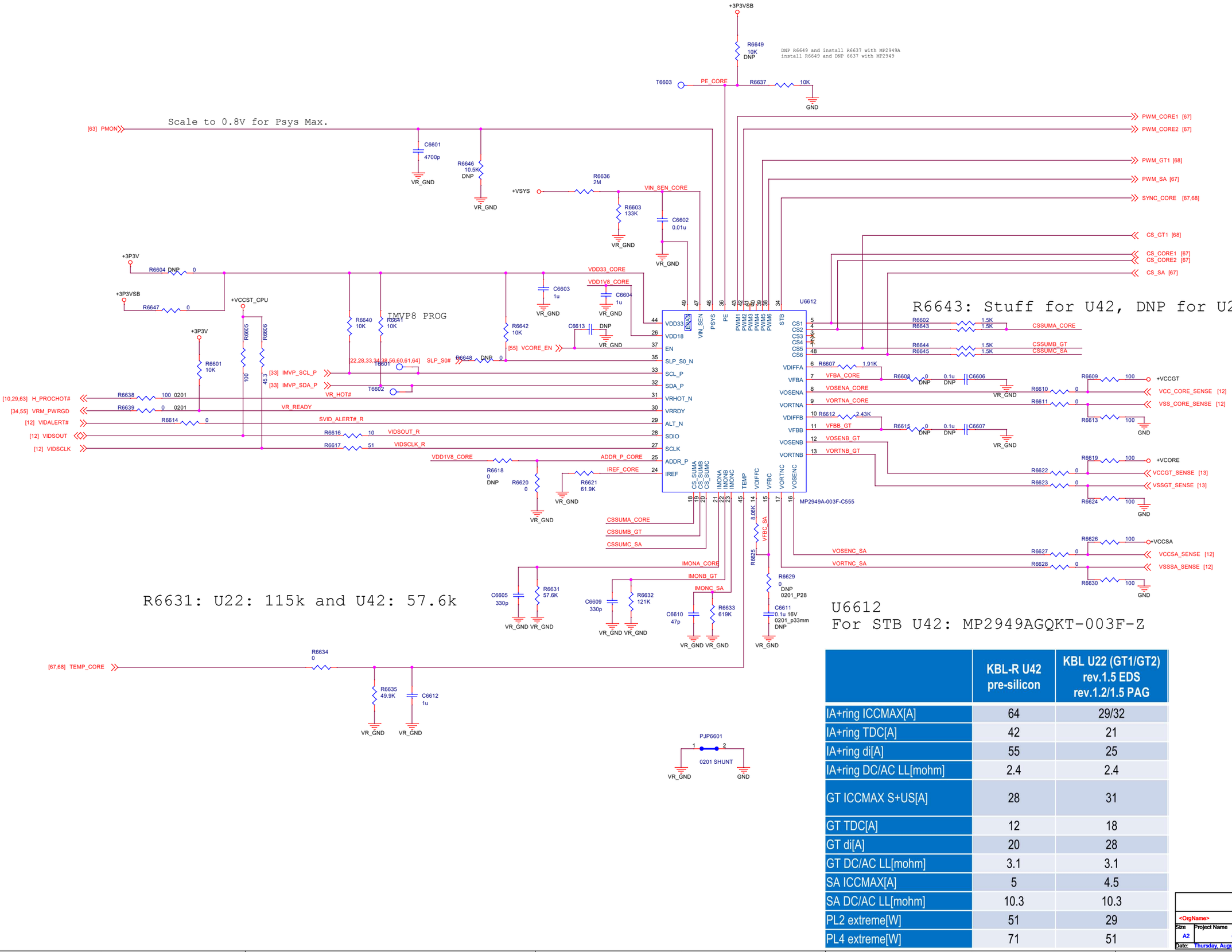
+5V_FAN
Imax=0.5A
07132016



Title:	+5V Load SW	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 64 of 76	

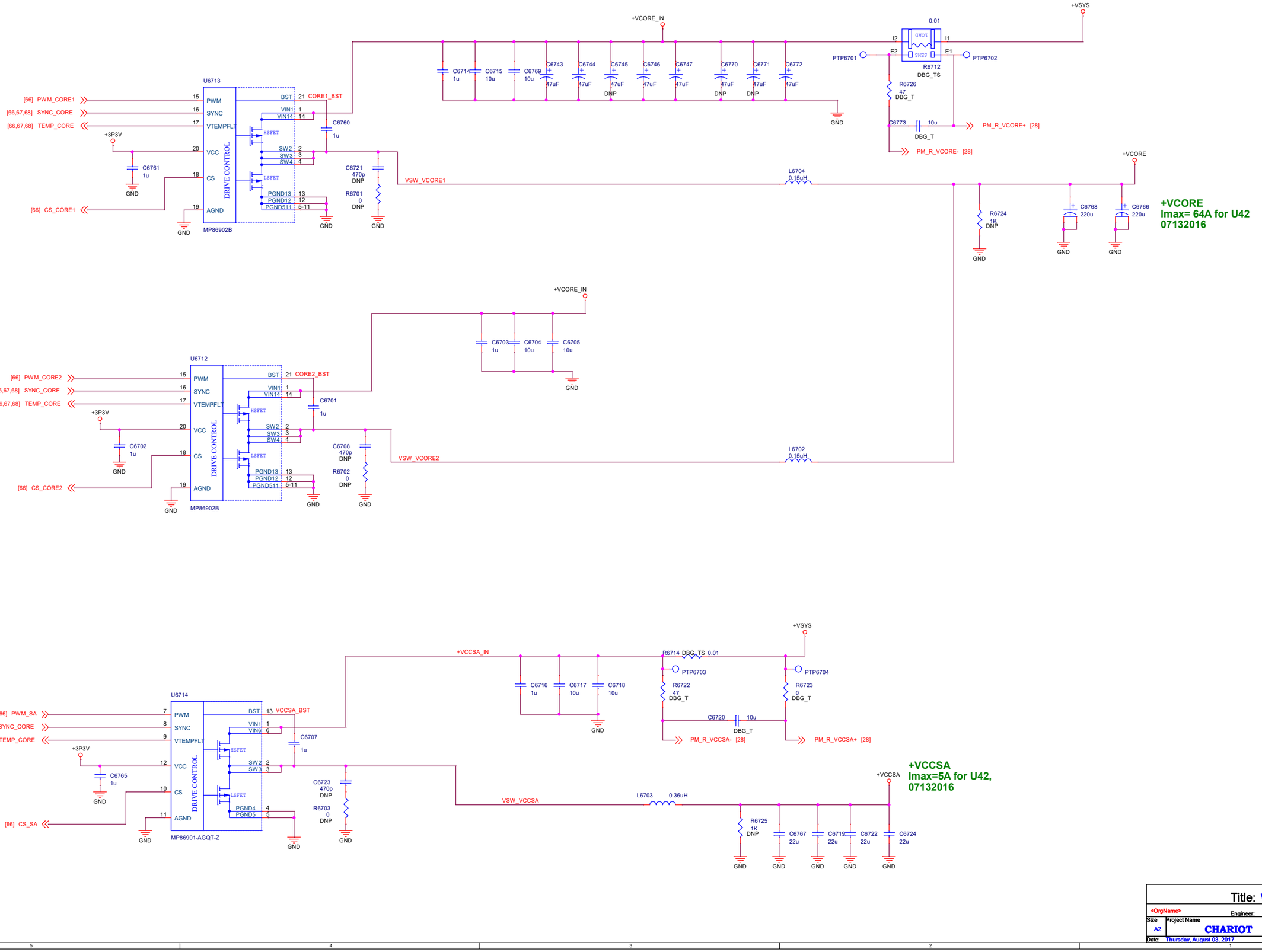


Title:	+3P3V Load SW		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 65 of 76		

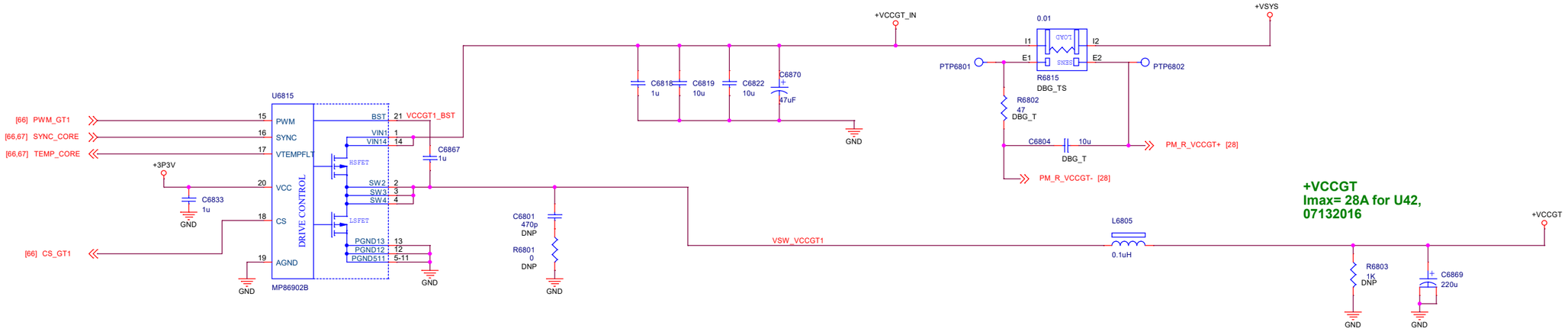


	KBL-R U42 pre-silicon	KBL U22 (GT1/GT2) rev.1.5 EDS rev.1.2/1.5 PAG
IA+ring ICCMAX[A]	64	29/32
IA+ring TDC[A]	42	21
IA+ring di[A]	55	25
IA+ring DC/AC LL[mohm]	2.4	2.4
GT ICCMAX S+US[A]	28	31
GT TDC[A]	12	18
GT di[A]	20	28
GT DC/AC LL[mohm]	3.1	3.1
SA ICCMAX[A]	5	4.5
SA DC/AC LL[mohm]	10.3	10.3
PL2 extreme[W]	51	29
PL4 extreme[W]	71	51

Title: VCPU contoller
<OrgName> Engineer: <OrgAddr1>
Size: A2 Project Name: CHARIOT Rev: 1.00
Date: Thursday, August 03, 2017 Sheet 66 of 76



Title: VCORE VCCSA			
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 67 of 76		



Title:	VCVGT		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 68 of 76		

Title:			X	
<OrgName>	Engineer:		<OrgAddr1>	
Size: A3	Project Name: CHARIOT			Rev: 1.00
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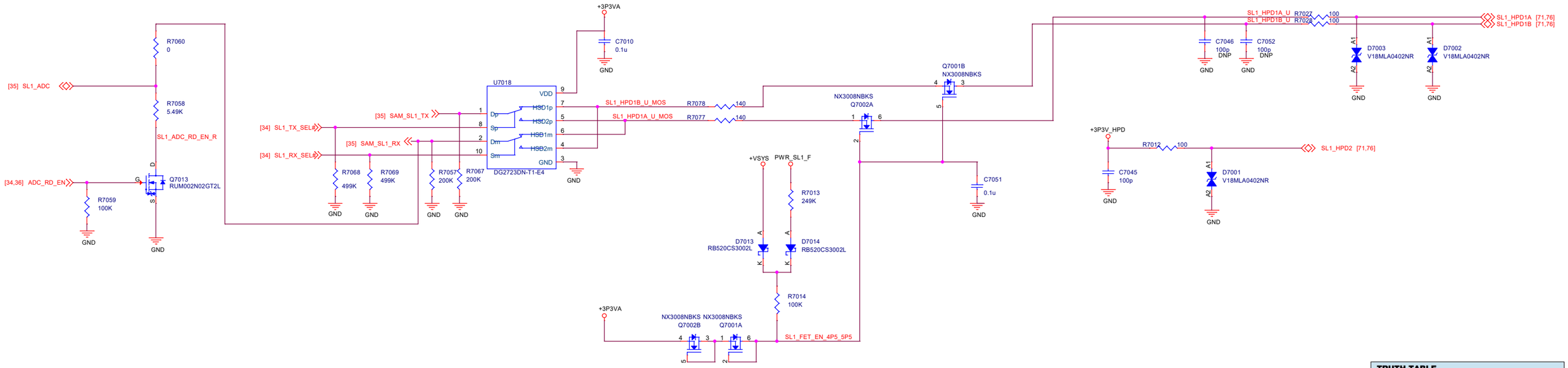
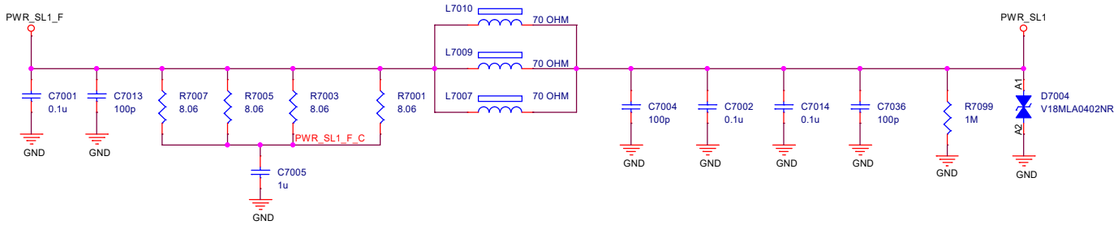
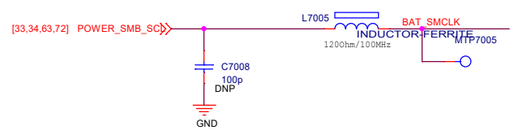
HPD FOR SL1 (ONE/TWO WIRE UART)

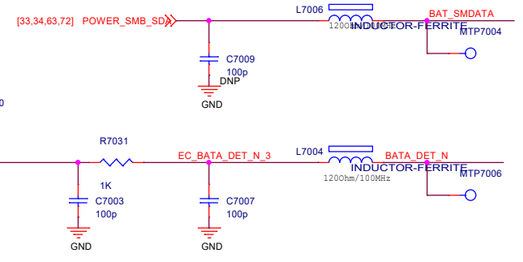




Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

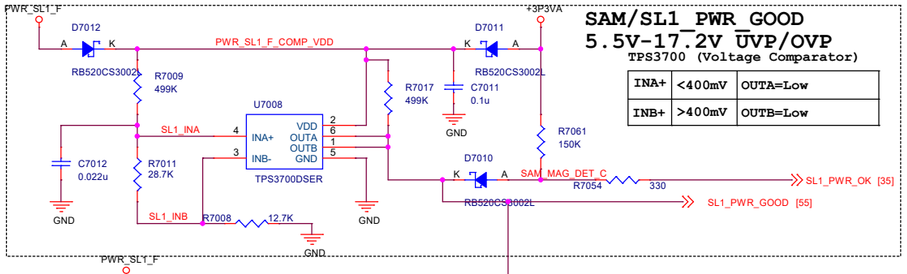




TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

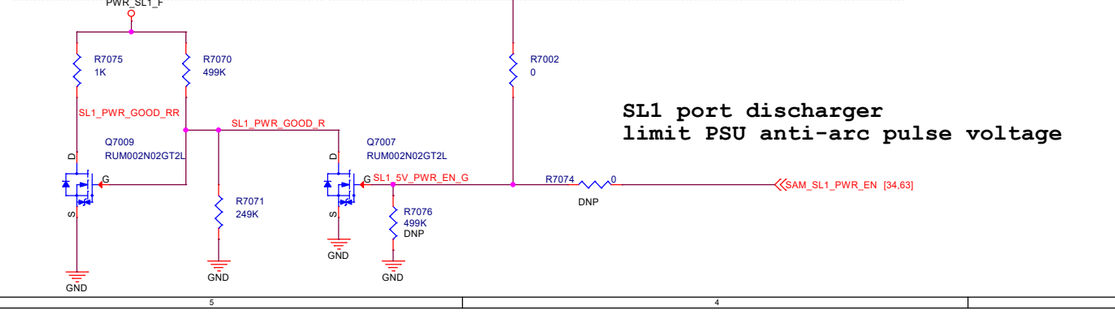
Base Battery lowest voltage



SAM/SL1_PWR_GOOD 5.5V-17.2V UVP/OVP

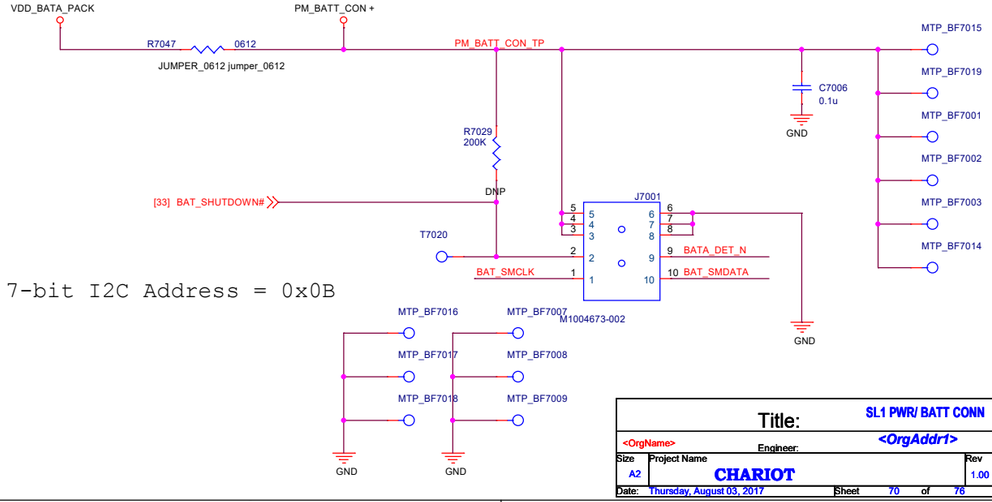
TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low



SL1 port discharger limit PSU anti-arc pulse voltage

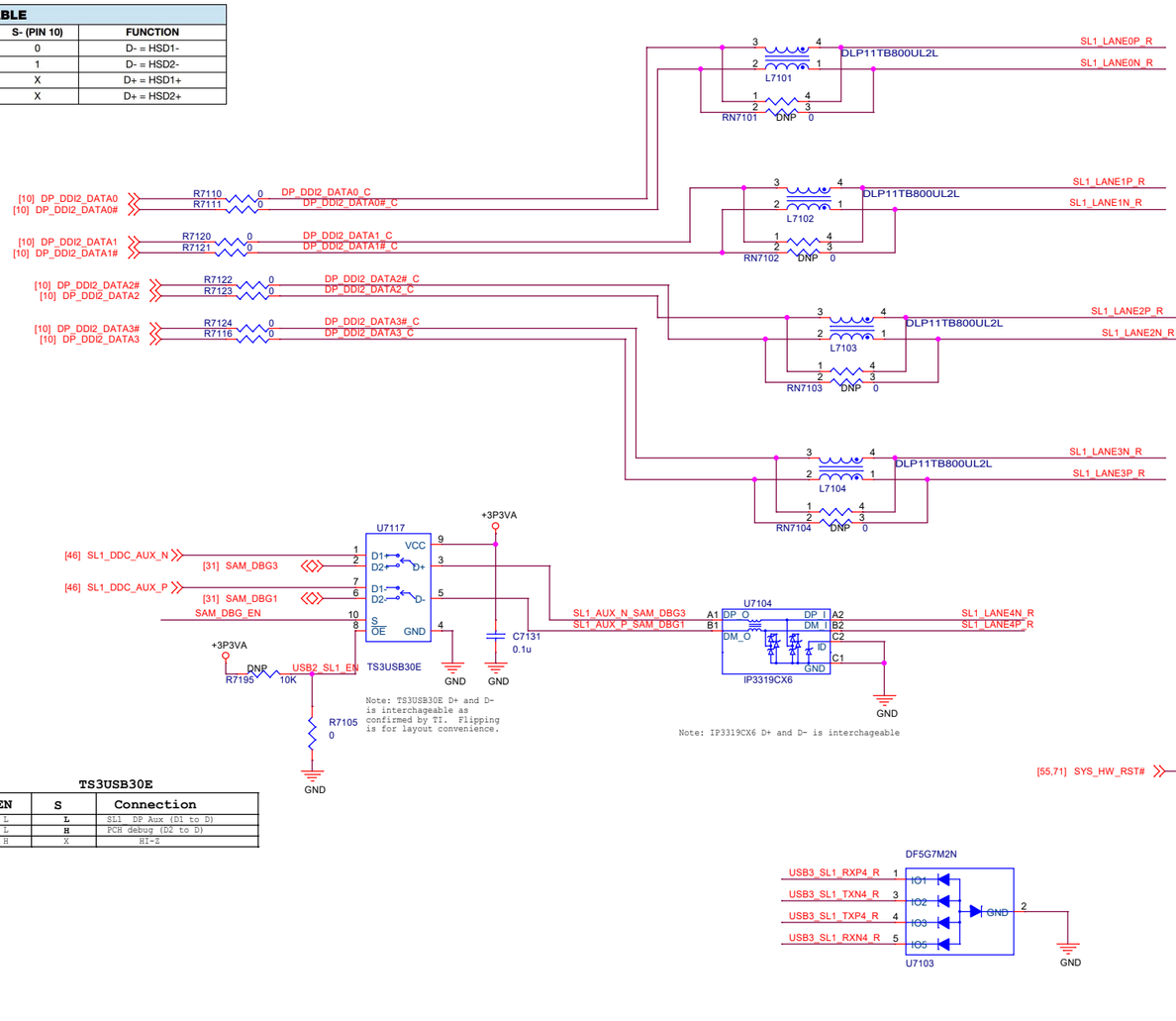
18W Battery Connector



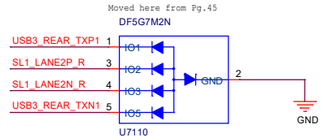
7-bit I2C Address = 0x0B

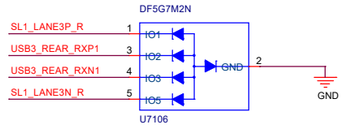
Title:	SL1 PWR/ BATT CONN
<OrgName>	Engineer: <OrgAddr1>
Size: A2	Project Name: CHARIOT
Rev: 1.00	
Date: Thursday, August 03, 2017	Sheet 70 of 76

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+



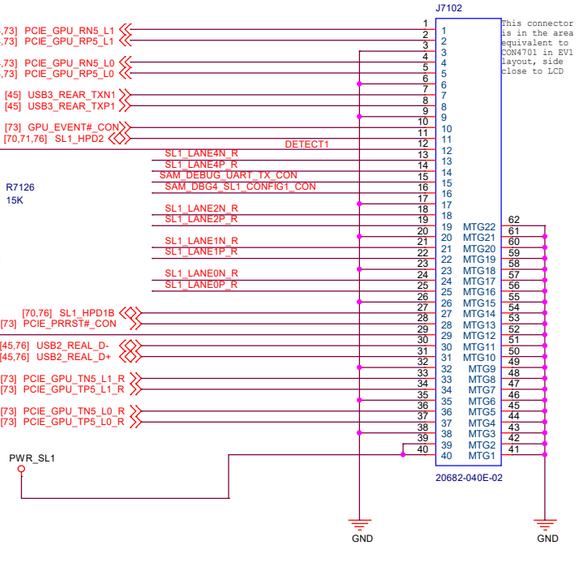
Moved here from Pg.45

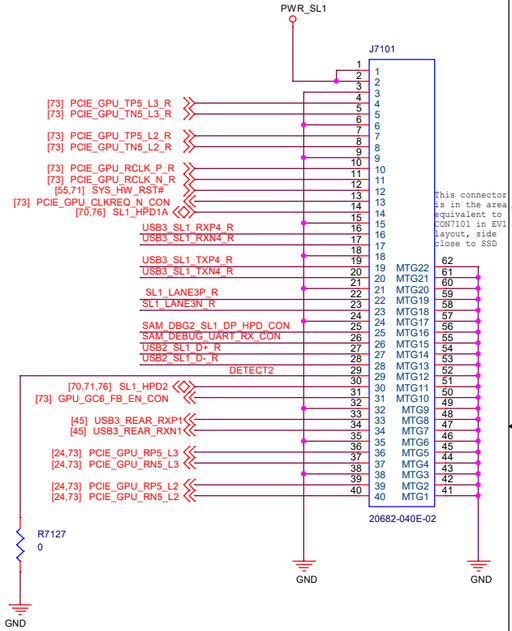


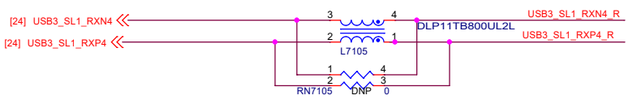


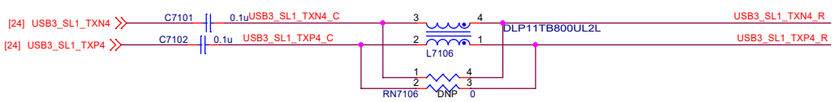
TS3USB30E

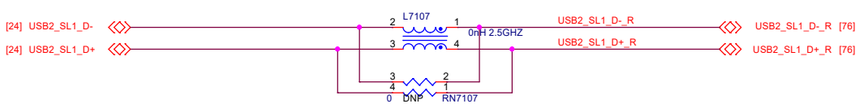
EN	S	Connection
L	L	SL1 DP Aux (D1 to D)
L	H	PCH debug (D2 to D)
H	X	HI-Z

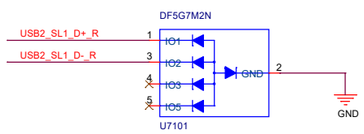






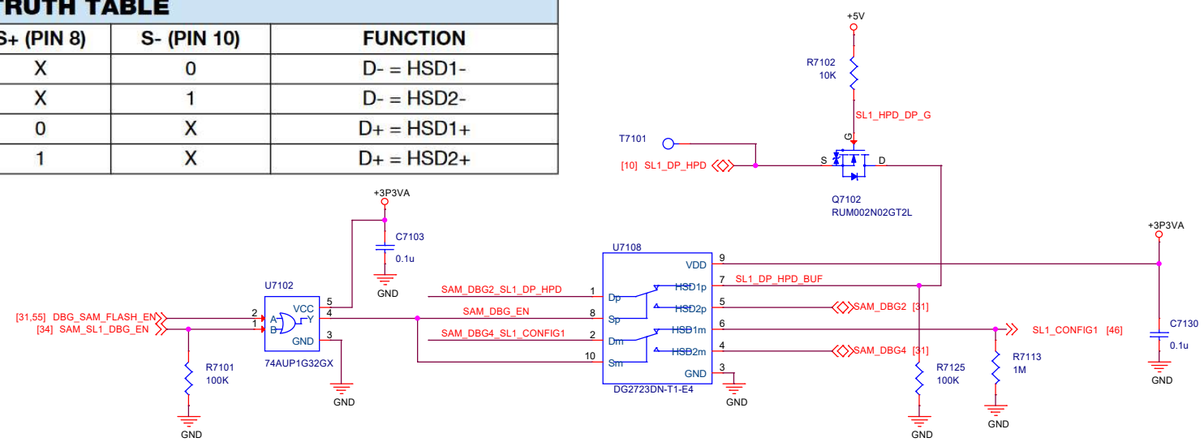






DG2723 Truth Table

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+



Title:	SL1 SINGNALS		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
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+3P3V_HPD
Imax=165uA
07132016

+VCC_EDP_BKLT_OUT
Imax=0.16A
07132016

+3P3VA
R7202
TR0603mils, NOTmm
PTP7202
DBG_S
PTP7201
C7201
1u
GND
+3P3V_HPD_VIN
+3P3VA
R7201
499K
+3P3V_HDP_EN
[34] SL1_HPD2_EN#
Q7201
RUM002N02GT2L
R7206
499K
GND
R7204
20K
+3P3V_HPD_ILIMIT
U7201
VIN_A1 VOUT_A3
VIN_B1 VOUT_B3
ON OCFLAGB
GND_A2 GND_B2
ISET
FPF2495UCX
+3P3V_HPD_OCFLAG
T7204
+3P3V_HPD
C7202
1u
R7239
499K
GND

+VCC_EDP_BKLT_IN
L7201
10uH
BKLT_SW
C7210
10u
C7213
10u
C7205
10u
C7209
0.1u
BKLT_BST_SW
+VCC_EDP_BKLT_OUT
C7206
2.2u
50V
C7207
2.2u
50V
C7208
2.2u
50V

+VCC_EDP_BKLT_IN
R7207
10
R7227
10K
DBG_D
C7218
1u
+VCC_BKLT
C7204
1u
U7202
VCC
VIN
PWM
EN
A0
A1
SCL
SDA
FT
AGND_EP
OUT
SW
BST
LED8
LED7
LED6
LED5
LED4
LED3
LED2
LED1
NC22
NC19
NC17
PGND
MP3376AGR-0002
L_BKLT_CTRL_R
R7209
1K
BKLT_PWM_R
MTP7202
MTP7203
BKLT_EN_R
R7208
1K
BKLT_EN
R7229
47
BKLT_BST
BKLT_FB8_R R7231
BKLT_FB7_R R7230
BKLT_FB6_R R7223
BKLT_FB5_R R7222
BKLT_FB4_R R7221
BKLT_FB3_R R7220
BKLT_FB2_R R7219
BKLT_FB1_R R7218
0
BKLT_FB8 [57,76]
BKLT_FB7 [57,76]
BKLT_FB6 [57,76]
BKLT_FB5 [57,76]
BKLT_FB4 [57,76]
BKLT_FB3 [57,76]
BKLT_FB2 [57,76]
BKLT_FB1 [57,76]
[33,34,63,70] POWER_SMB_SCL
SSM6N15AFU
Q7204A
DBG_D
[33,34,63,70] POWER_SMB_SDA
SSM6N15AFU
Q7204B
DBG_D
BKLT_SCL
BKLT_SDA

[28] PM_R_EDPBLKT+
C7221
10u
DBG_T
PM_R_EDPBLKT- [28]
R7235
0
DBG_T
R7234
47
DBG_T
PTP7204
+VCC_EDP_BKLT_IN
+VSYS
Q7203
IRLML6402
+VCC_EDP_BKLT_IN_REG
PTP7203
R7217
0.01
DBG_TS
R7213
100K
C7215
1000p
+VCC_EDP_BKLT_IN_DRI
C7216
0.1u
DNP
R7216
5.1K
R7215
5.1K
R7214
200K
Q7202B
SSM6N15AFU
+VCC_EDP_BKLT_IN_DISC
Q7202A
SSM6N15AFU
+VCC_EDP_BKLT_IN_DRI_R
+3P3V_PANEL
R7211
22K
+VCC_EDP_BKLT_IN_R
R7212
100K
C7214
0.1u
DNP

7-bit I2C Address = 0x28

+3P3VSB
C7220
0.1u
U7204
VDD
HSD1p
HSD2p
HSD1m
HSD2m
GND
Dp
Sp
Dm
Sm
DG2723DN-T1-E4
[34] PANEL_LOGO_BKLT_EN
[10] L_BKLTEN
[34] PANEL_LOGO_PWM
[10] L_BKLT_CTRL
BKLT_EN_R
L_BKLT_CTRL_R
R7237
0
BL_INST_ON_HNKSHK [10,35]
R7205
100K
R7236
47K

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

Title: +3P3V_HPD/LCD backlight
<OrgName>
Engineer: <OrgAddr1>
Size A3
Project Name CHARIOT
Rev 1.00
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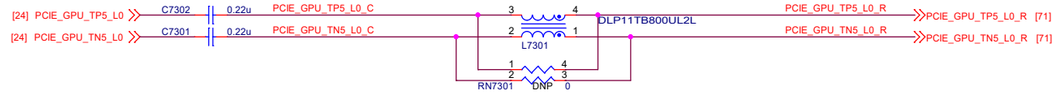
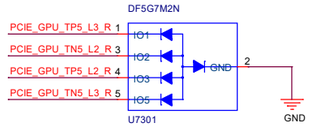
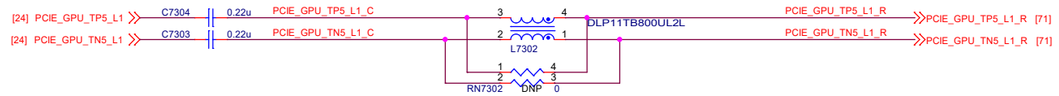
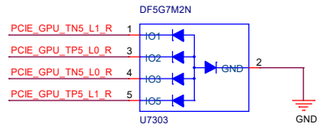
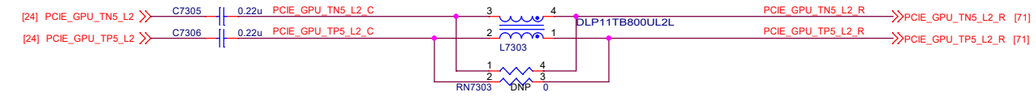
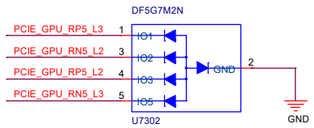


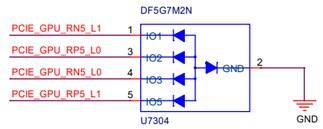


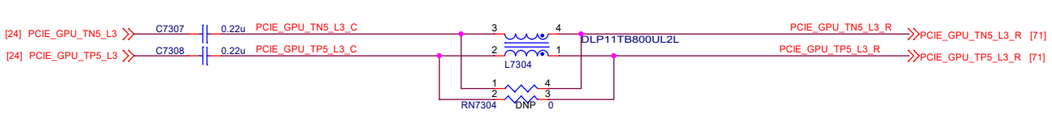


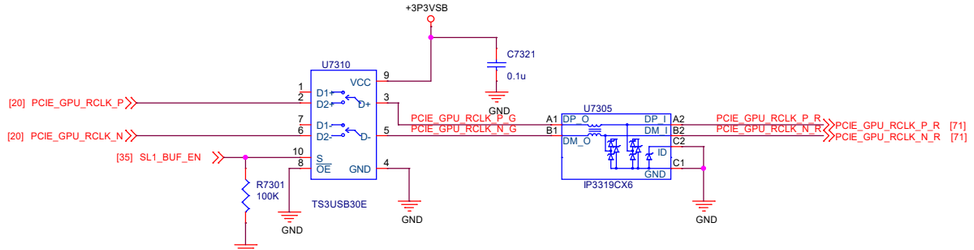






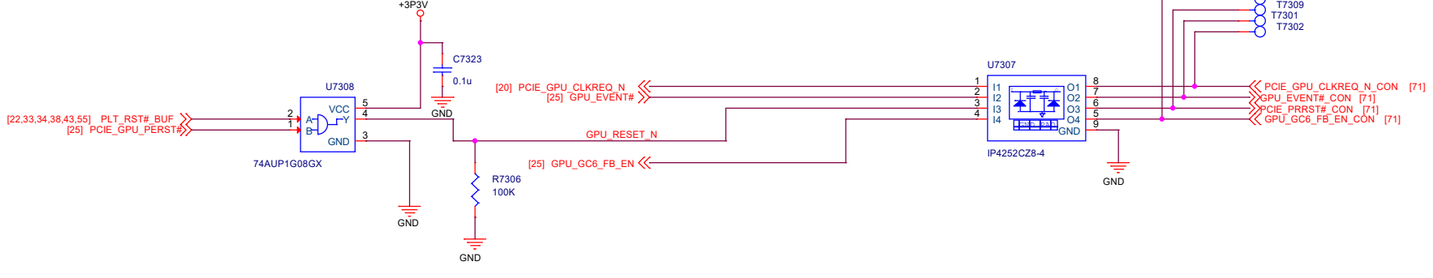






TS3USB30E

EN	S	Connection
L	L	(D1 to D)
L	H	(D2 to D)
H	X	HI-Z



Title:	PCIe GPU		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: CHARIOT		Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 73 of 76		

Title: X				
<OrgName>	Engineer:		<OrgAddr1>	
Size: Custom	Project Name: CHARIOT			Rev: 1.00
Date: Thursday, August 03, 2017		Sheet 74 of 76		

Title:	X			
<OrgName>	Engineer:	<OrgAddr1>		
Size: A3	Project Name: CHARIOT			Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 75 of 76			

+VCC_EDP_BKLT_OUT MTP7601
+1P8V MTP7615
+VCC_RTC MTP7608
+3P3VA MTP_BF7602
+5V_AUDIO MTP7616
+3P3V MTP7609
+3P3VSB MTP7603
+3P3V_ACC MTP7610
+5VSB MTP_BF7604
+1P8V_DUAL MTP7618
+3P3V_WWAN MTP7681
+5V MTP7605
+3P3V_SSD MTP7687
+3P3V_PANEL MTP7685
+1VSB MTP7679
+1P8VSB MTP7607
+1P8V_AUDIO MTP7665
+VCCIO MTP7662
+3P3VAS MTP76124
+1P8V_TS MTP7666
+VCCST_CPU MTP7661
+VCCSTG MTP7659
+VCCGT MTP7652
+VCCSA MTP7657

[45,71] USB2_REAL_D- MTP_BF7637
[45,71] USB2_REAL_D+ MTP_BF7638
MTP_BF7640
GND
[71] USB2_SL1_D+_R MTP_BF7667
[71] USB2_SL1_D-_R MTP_BF7668
[41] DMIC1_CLK_R T7641
[41] DMIC1_DATA_R T7699
[41] DMIC_PWR MTP_BF7643
MTP7644
GND

+3P3V_HPD MTP7683
+5V_TS MTP7692

+1P2V_CAM_R MTP76135
+2P8V_CAM_R MTP76136
+2P8V_CAM_IR MTP76137
+2P8V_CAM_F MTP76132
+1P8V_CAM_R MTP76140
+1P8V_CAM_IR MTP76141
+1P8V_CAM_F MTP76142

PWR_SL1
MTP_BF7670 MTP_BF7656
MTP_BF7653 MTP_BF7671
MTP_BF7654 MTP_BF7672
MTP_BF7655 MTP_BF7673
MTP_BF76105 MTP_BF76104
MTP_BF76103 MTP_BF76102
GND

MTP76101
[70,71] SL1_HPD2
MTP7682
[70,71] SL1_HPD1B
MTP7684
[70,71] SL1_HPD1A

+1P2V_DUAL MTP7611
+V_VDDQ_VTT MTP7612
+VCORE MTP_BF7613
+VDDQ_VREF T7614
+VCCPLL_OC MTP7651

[41] MIC1_CR_F_C MTP7625
MTP7626
GND
[41] HPOUT_L_F_C MTP7627
[41] HPOUT_R_F_C MTP7628
[40,41] HPOUT_JD MTP7674
close to CON4101

[39] CFAN_PWM_R_1 MTP7645
[39] CFAN_D_1 MTP7646
+5V_FAN MTP7648
MTP7647
GND
close to J3901

+3P3V_VCM MTP76149

MTP7642 BKLT_FB1 [57,72]
MTP7650 BKLT_FB2 [57,72]
MTP7680 BKLT_FB3 [57,72]
MTP7606 BKLT_FB4 [57,72]
MTP7677 BKLT_FB5 [57,72]
MTP7678 BKLT_FB6 [57,72]
MTP76148 BKLT_FB8 [57,72]
MTP76147 BKLT_FB7 [57,72]

MTP7631
AGND
close to audio

T7634
GND
close to CON4901

[30,33] VOL_UP_R MTP_BF7632
[30,33] VOL_DOWN_R MTP_BF7633
close to CON4101

[30,33] PWR_SW# MTP_BF7635
MTP_BF7636
GND
close to CON3003

[39] CFAN_PWM_R_2 MTP76131
[39] CFAN_D_2 MTP76130
close to J3902

MTP7621
[41] SPKR+_CON
MTP7622
[41] SPKR-_CON
MTP7623
[41] SPKL+_CON
MTP7624
[41] SPKL-_CON
close to speaker connector

Title:	Test Point	
<OrgName>	Engineer:	<OrgAddr1>
Size: A3	Project Name: CHARIOT	Rev: 1.00
Date: Thursday, August 03, 2017	Sheet 76 of 76	